9–4 THE 555 TIMER

One of the most versatile linear integrated circuits is the 555 timer. Signetics Corporation first introduced this device as the SE/NE 555 in early 1970. Since its debut, the device has been used in a number of novel and useful applications. A sample of these applications includes monostable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control devices, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others. The 555 is a monolithic timing circuit that can produce accurate and highly stable time delays or oscillation. The timer basically operates in one of two modes: either as a monostable (one-shot) multivibrator or as an astable (free-running) multivibrator. The device is available as an 8-pin metal can, an 8-pin mini DIP, or a 14-pin DIP. Figure 9–15 shows the connection diagram and the block diagram of the SE/NE 555 timer. The SE555 is designed for the operating temperature range from −55° to +125°C, while the NE555 operates over a temperature range of 0° to +70°C. The important features of the 555 timer are these: it operates on +5 to +18 V supply voltage in both free-running (astable) and one-shot (monostable) modes; it has an adjustable duty cycle; timing is from microseconds through hours; it has a high current output; it can source or sink 200 mA; the output can drive TTL and has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature, or equivalently 0.005%/°C. Like general-purpose op-amps, the 555 timer is reliable, easy to use, and low cost.

The next several sections explain the operation of the 555 timer as a monostable and astable multivibrator; a few simple applications using these two modes are then presented.

9–4–1 The 555 as a Monostable Multivibrator

A monostable multivibrator, often called a *one-shot* multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the *RC* network connected externally to the 555 timer. In a stable or standby state the output of the circuit is approximately zero or at logic-low level. When an external trigger pulse is applied, the output is forced to go *high* ($\cong V_{CC}$). The time the output remains high is determined by the external *RC* network connected to the timer. At the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (output low), hence the name *monostable*. Normally, the output of the monostable multivibrator is low.

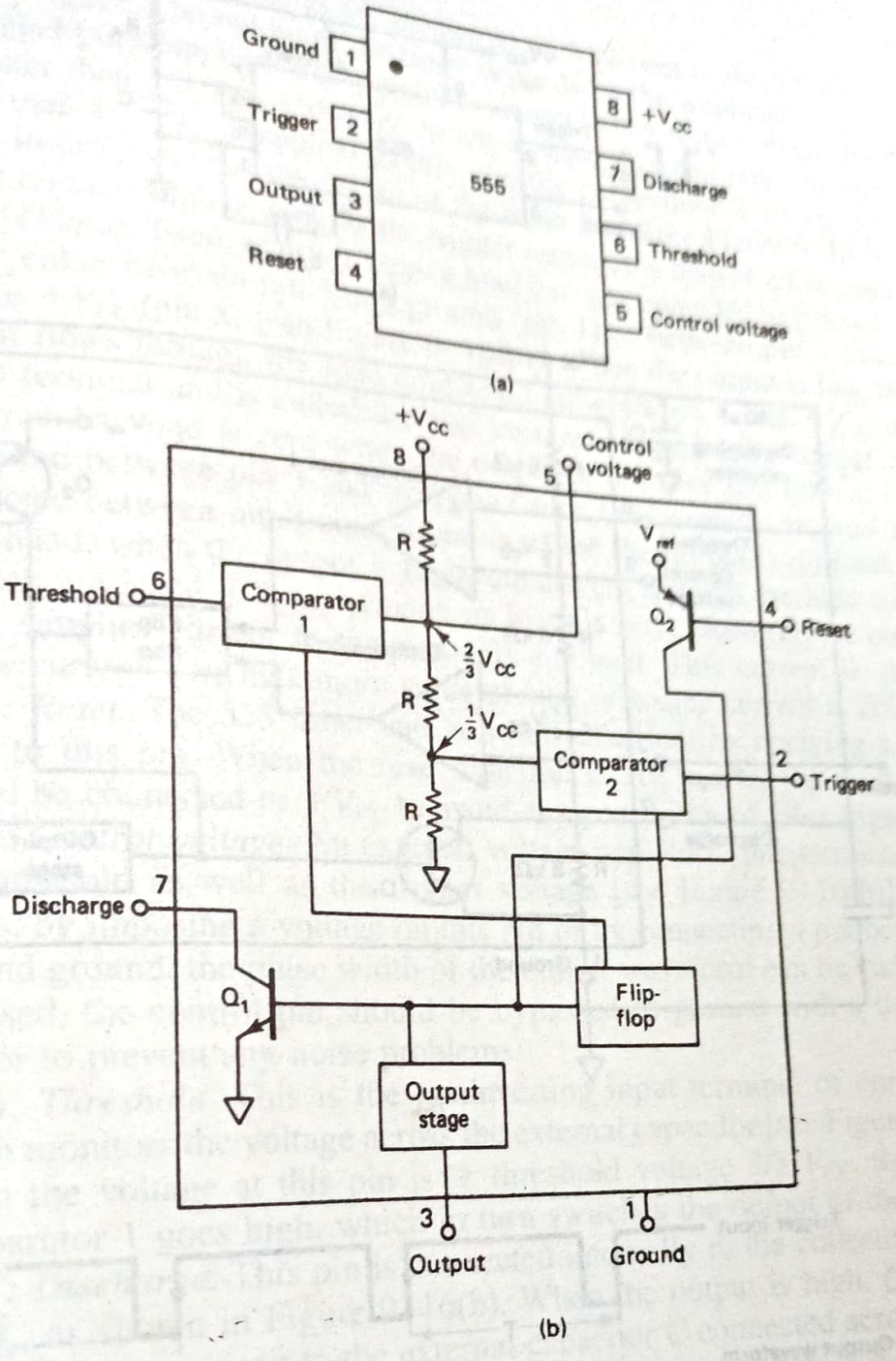


FIGURE 9–15 (a) 555 timer connection diagram. (b) Block diagram. (Courtesy of Signetics Corporation.)

Figure 9–16(a) shows the 555 configured for monostable operation. To better explain the circuit's operation, the internal block diagram is included in Figure 9–16(b).

Before proceeding with the operation of the 555 timer as a monostable multivibrator, it is important to examine its pin functions. The pin numbers used in the following discussion refer to the 8-pin mini DIP and 8-pin metal can packages [see Figure 9–15(a)].

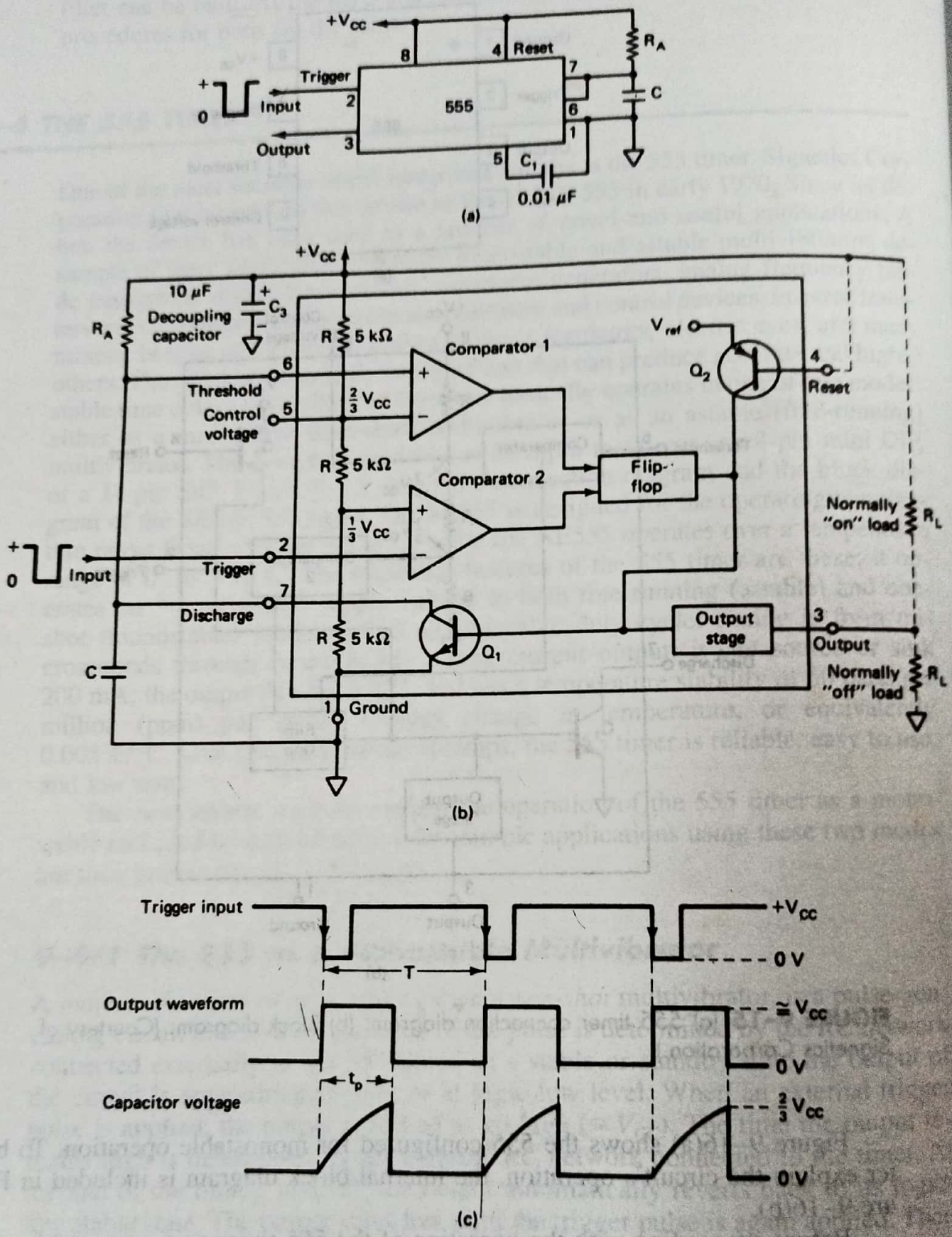


FIGURE 9–16 (a) and (b) 555 connected as a monostable multivibrator. (c) Input and output waveforms.

Pin 1: Ground. All voltages are measured with respect to this terminal.
Pin 2: Trigger. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin. The output is low if the voltage at this pin is greater than 2/3 V_{CC}. However, when a negative-going pulse of amplitude larger than 1/3 V_{CC} is applied to this pin, the comparator 2 output goes low, which in turn switches the output of the timer high [see Figure 9–15(b)]. The output remains high as long as the trigger terminal is held at a low voltage.
Pin 3: Output. There are two ways a load can be connected to the output terminal: either between pin 3 and ground (pin 1) or between pin 3 and supply voltage $+V_{CC}$ (pin 8) [see Figure 9–16(b)]. When the output is low, the load current flows through the load connected between pin 3 and $+V_{CC}$ into the output terminal and is called the *sink* current. However, the current through the grounded load is zero when the output is low. For this reason, the load connected between pin 3 and $+V_{CC}$ is called the *normally on load* and that connected between pin 3 and ground is called the *normally off load.* On the other hand, when the output is high, the current through the load connected between pin 3 and $+V_{CC}$ (normally on load) is zero. However, the output terminal supplies current to the normally off load. This current is called the *source* current. The maximum value of sink or source current is 200 mA.
Pin 4: Reset. The 555 timer can be reset (disabled) by applying a negative pulse to this pin. When the reset function is not in use, the reset terminal should be connected to $+V_{CC}$ to avoid any possibility of false triggering.
Pin 5: Control voltage. An external voltage applied to this terminal changes the threshold as well as the trigger voltage [see Figure 9–16(b)]. In other words, by imposing a voltage on this pin or by connecting a pot between this pin and ground, the pulse width of the output waveform can be varied. When not used, the control pin should be bypassed to ground with a 0.01-μF capacitor to prevent any noise problems.
Pin 6: Threshold. This is the noninverting input terminal of comparator 1, which monitors the voltage across the external capacitor [see Figure 9–16(b)]. When the voltage at this pin is $\geq$ threshold voltage 2/3 V_{CC}, the output of comparator 1 goes high, which in turn switches the output of the timer low.
Pin 7: Discharge. This pin is connected internally to the collector of transistor Q_1, as shown in Figure 9–16(b). When the output is high, Q_1 is off and acts as an open circuit to the external capacitor C connected across it. On the other hand, when the output is low, Q_1 is saturated and acts as a short circuit, shorting out the external capacitor C to ground.
Pin 8: $+V_{CC}$. The supply voltage of +5 V to +18 V is applied to this pin with respect to ground (pin 1).

9–4–1(a) Monostable operation.

According to Figure 9–16(b), initially when the output is low, that is, the circuit is in a stable state, transistor Q_1 is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q_1 is turned off, which releases the short circuit across the external capacitor C and

drives the output high. The capacitor C now starts charging up toward V_{CC} through R_A. However, when the voltage across the capacitor equals 2/3 V_{CC}, comparator 1's output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q_1 on, and hence capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats. Figure 9–16(c) shows the trigger input, output voltage, and capacitor voltage waveforms. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also, the trigger pulse must be a negative-going input signal with an amplitude larger than 1/3 V_{CC}.

The time during which the output remains high is given by

$$t_p = 1.1R_AC \quad \text{seconds} \tag{9–7}$$

where R_A is in ohms and C is in farads. Figure 9–17 shows a graph of the various combinations of R_A and C necessary to produce desired time delays. Note that

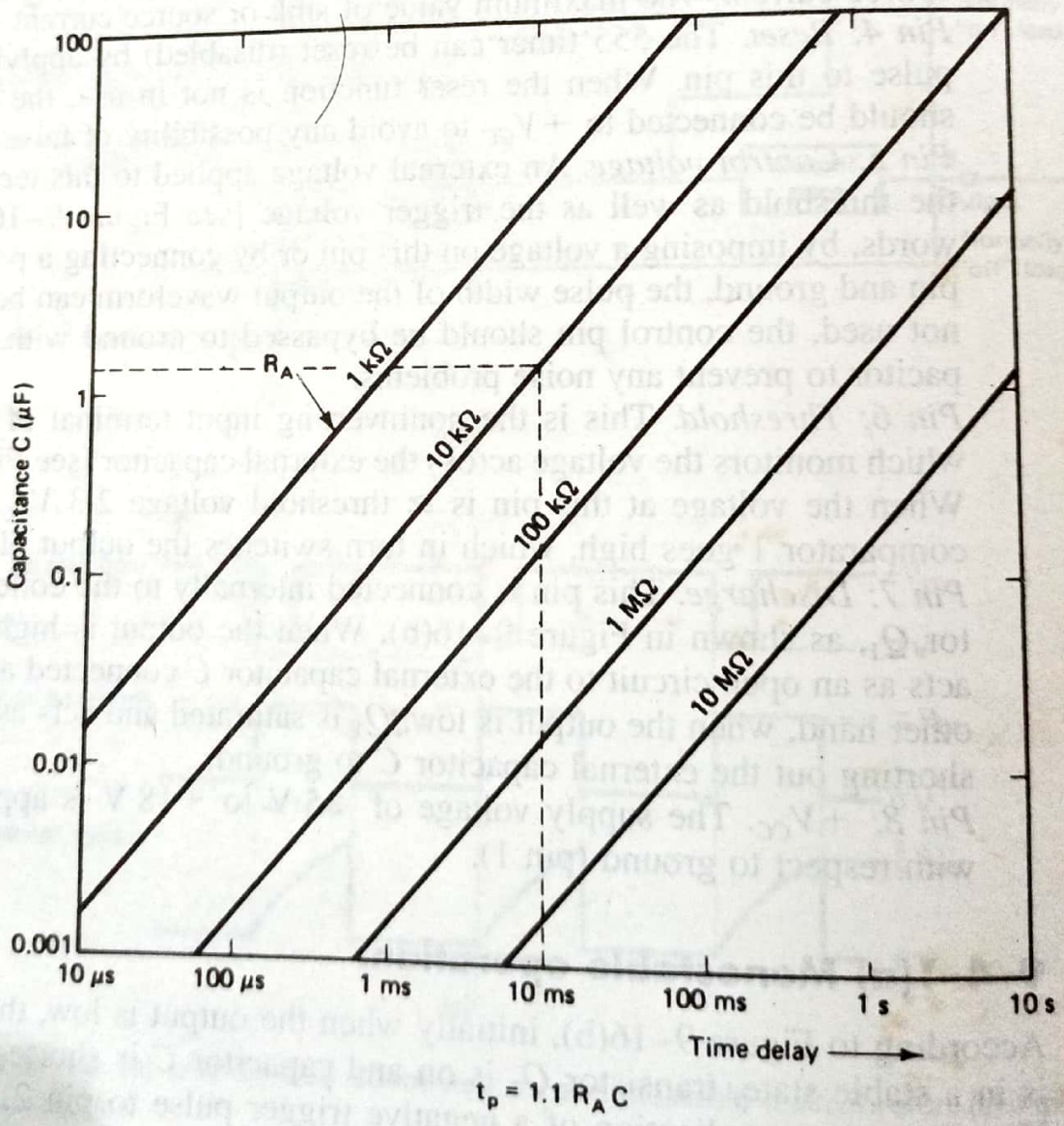


FIGURE 9–17 Determining R_A and C values for various time delays.

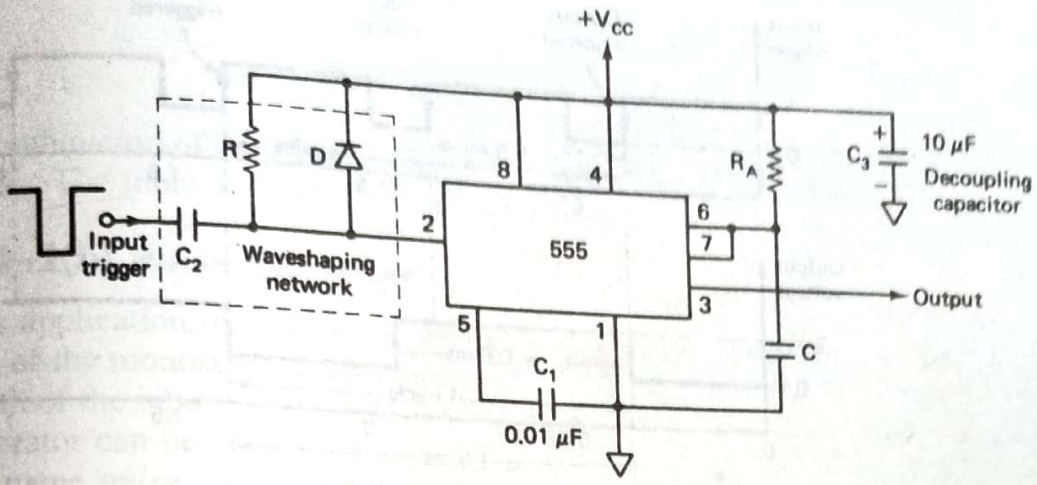


FIGURE 9–18 Monostable multivibrator with waveshaping network to prevent positive pulse edge triggering.

this graph can only be used as a guideline and gives only the approximate values of R_A and C for a given time delay.

Once triggered, the circuit's output will remain in the high state until the set time t_p elapses. The output will not change its state even if an input trigger is applied again during this time interval t_p. However, the circuit can be reset during the timing cycle by applying a negative pulse to the reset terminal. The output will then remain in the low state until a trigger is again applied.

Often in practice a decoupling capacitor (10 μF) is used between $+V_{CC}$ (pin 8) and ground (pin 1) to eliminate unwanted voltage spikes in the output waveform. Sometimes, to prevent any possibility of mistriggering the monostable multivibrator on positive pulse edges, a waveshaping circuit consisting of R, C_2, and diode D is connected between the trigger input pin 2 and V_{CC} pin 8, as shown in Figure 9–18. The values of R and C_2 should be selected so that the time constant RC_2 is smaller than the output pulse width t_p.

EXAMPLE 9–5

In the circuit of Figure 9–16(a), $R_A = 10\ \text{k}\Omega$, the output pulse width $t_p =$ 10 ms. Determine the value of C.

SOLUTION

Rearranging Equation (9–7), we get

$$C = \frac{(10)(10^{-3})}{(1.1)(10^4)} = 0.909\ \mu\text{F} \cong 1\ \mu\text{F}$$

(Notice that approximately the same value can be obtained for C from the time delay graph of Figure 9–17.)

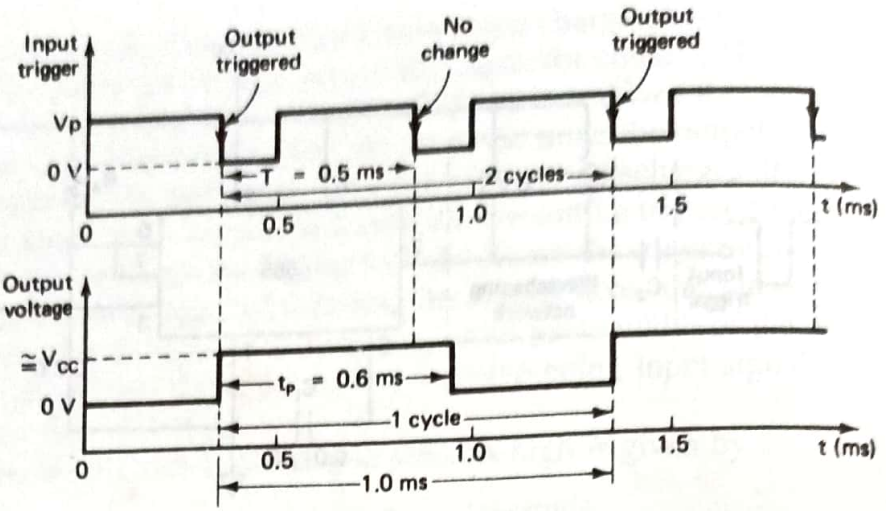


FIGURE 9–19 Input and output waveforms of the monostable multivibrator as a divide-by-2 network.

9–4–2 Monostable Multivibrator Applications

9–4–2(a) Frequency divider

The monostable multivibrator of Figure 9–16(a) can be used as a frequency divider by adjusting the length of the timing cycle t_p with respect to the time period T of the trigger input signal applied to pin 2. To use the monostable multivibrator as a divide-by-2 circuit, the timing interval t_p must be slightly larger than the time period T of the trigger input signal, as shown in Figure 9–19. By the same concept, to use the monostable multivibrator as a divide-by-3 circuit, t_p must be slightly larger than twice the period of the input trigger signal, and so on.

The frequency-divider application is possible because the monostable multivibrator cannot be triggered during the timing cycle.

EXAMPLE 9–6

The circuit of Figure 9–16(a) is to be used as a divide-by-2 network. The frequency of the input trigger signal is 2 kHz. If the value of $C = 0.01\ \mu F$, what should be the value of R_A?

SOLUTION

For a divide-by-2 network, t_p should be slightly larger than T. Let

$$t_p = 1.2T$$

Therefore,

$$t_p = (1.2)\frac{1}{2\text{ kHz}} = 0.6\text{ ms}$$

Rearranging Equation (9–7) yields

$$R_A = \frac{(0.6)(10^{-3})}{(1.1)(10^{-8})} = 54.5\ \text{k}\Omega$$

A combination of a 10-kΩ fixed resistor and a 50-kΩ potentiometer may be used for R_A. The input and output waveforms are shown in Figure 9–19.

9–4–2(b) Pulse stretcher

This application makes use of the fact that the output pulse width (timing interval) of the monostable multivibrator is of longer duration than the negative pulse width of the input trigger. As such, the output pulse width of the monostable multivibrator can be viewed as a stretched version of the narrow input pulse, hence the name *pulse stretcher*. Often, narrow-pulse-width signals are not suitable for driving an LED display, mainly because of their very narrow pulse widths. In other words, the LED may be flashing but not be visible to the eye because its *on* time is infinitesimally small compared to its *off* time. The 555 pulse stretcher can be used to remedy this problem.

Figure 9–20 shows a basic monostable used as a pulse stretcher with an LED indicator at the output. The LED will be on during the timing interval $t_p = 1.1R_AC$, which can be varied by changing the value of R_A and/or C.

9–4–3 The 555 as an Astable Multivibrator

An astable multivibrator, often called a *free-running* multivibrator, is a rectangular-wave-generating circuit. Unlike the monostable multivibrator, this circuit does not require an external trigger to change the state of the output, hence the name *free-running*. However, the time during which the output is either high or low is determined by two resistors and a capacitor, which are externally connected to the 555 timer.

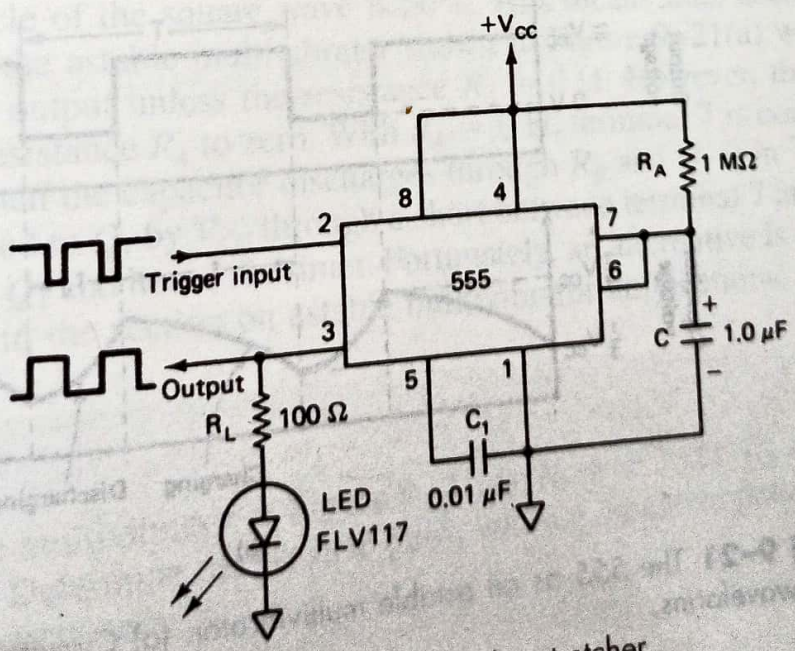


FIGURE 9–20 Monostable multivibrator as a pulse stretcher.

9–4–3(a) Astable operation

Figure 9–21(a) shows the 555 timer connected as an astable multivibrator. Initially, when the output is high, capacitor C starts charging toward V_{CC} through R_A and R_B. However, as soon as voltage across the capacitor equals 2/3 V_{CC}, comparator 1 triggers the flip-flop, and the output switches low [see Figure 9–21(b)]. Now capacitor C starts discharging through R_B and transistor Q_1. When the voltage across C equals 1/3 V_{CC}, comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage and capacitor voltage waveforms are shown in Figure 9–21(b).

As shown in this figure, the capacitor is periodically charged and discharged between 2/3 V_{CC} and 1/3 V_{CC}, respectively. The time during which the capacitor

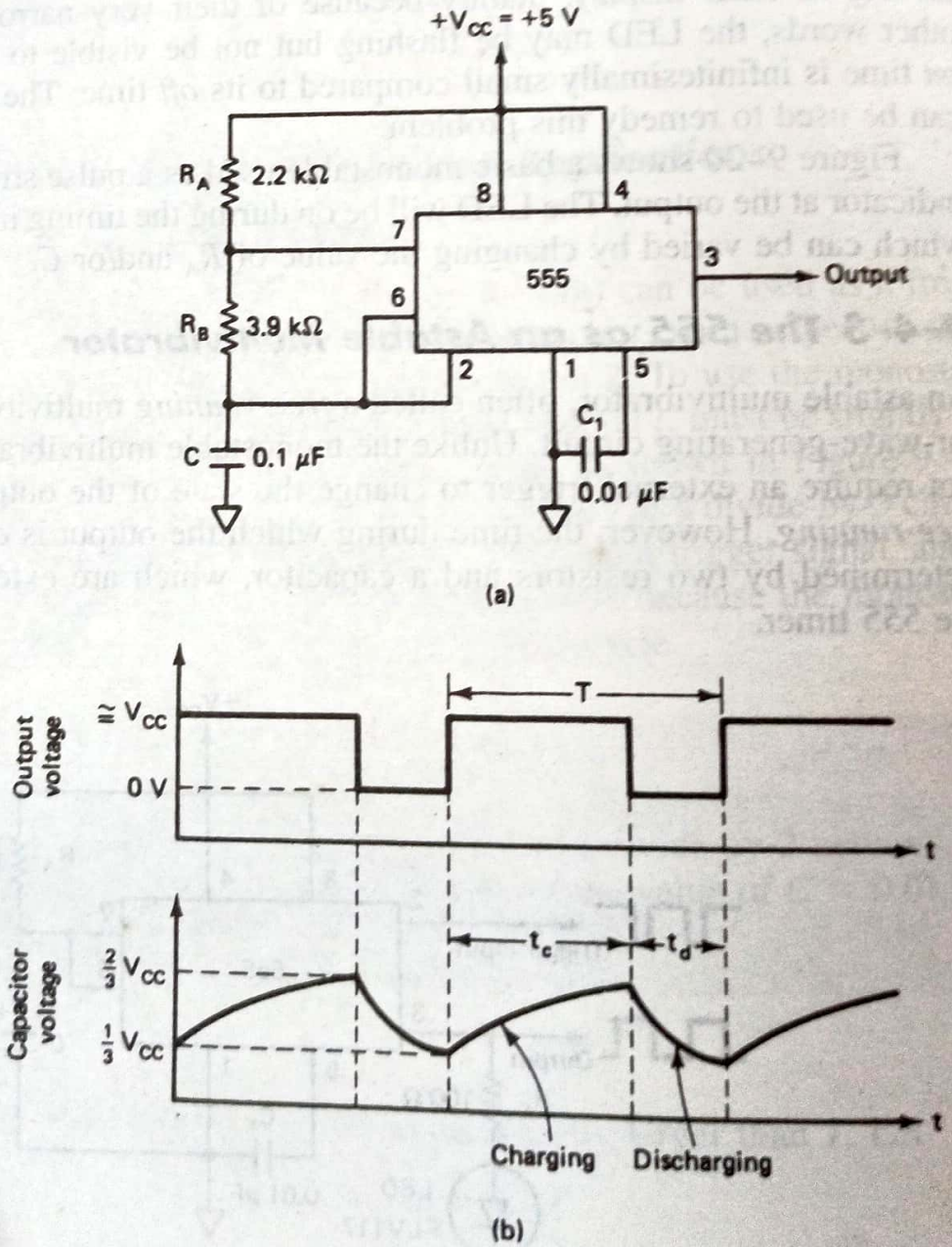


FIGURE 9–21 The 555 as an astable multivibrator. (a) Circuit. (b) Capacitor and output voltage waveforms.

charges from 1/3 V_{CC} to 2/3 V_{CC} is equal to the time the output is high and is given by

$$t_c = 0.69(R_A + R_B)C \tag{9–8a}$$

where R_A and R_B are in ohms and C is in farads. Similarly, the time during which the capacitor discharges from 2/3 V_{CC} to 1/3 V_{CC} is equal to the time the output is low and is given by

$$t_d = 0.69(R_B)C \tag{9–8b}$$

where R_B is in ohms and C is in farads. Thus the total period of the output waveform is

$$T = t_c + t_d = 0.69(R_A + 2R_B)C \tag{9–9}$$

This, in turn, gives the frequency of oscillation as

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{9–10}$$

Equation (9–10) indicates that the frequency f_o is independent of the supply voltage V_{CC}. The frequency of oscillation (free-running frequency) f_o can also be found by using Figure 9–22.

Often the term *duty cycle* is used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time t_c during which the output is high to the total time period T. It is generally expressed as a percentage. In equation form,

$$\% \text{ duty cycle} = \frac{t_c}{T} \times 100$$

$$= \frac{R_A + R_B}{R_A + 2R_B}(100) \tag{9–11}$$

The duty cycle of the square wave is 50%. This means that, according to Equation (9–11), the astable multivibrator shown in Figure 9–21(a) will not produce square-wave output unless the resistance $R_A = 0\ \Omega$. However, there is a danger in shorting resistance R_A to zero. With $R_A = 0\ \Omega$, terminal 7 is connected directly to $+V_{CC}$. When the capacitor discharges through R_B and Q_1 (pin 7), an extra current is supplied to Q_1 by V_{CC} through a short between terminal 7 and $+V_{CC}$, which may damage Q_1 and hence the timer. Fortunately, an alternative is available, which is explained in the section on astable multivibrator applications.

EXAMPLE 9–7

In the astable multivibrator of Figure 9–21(a), $R_A = 2.2\ \text{k}\Omega$, $R_B = 3.9\ \text{k}\Omega$, and $C = 0.1\ \mu\text{F}$. Determine the positive pulse width t_c, negative pulse width t_d, and free-running frequency f_o.

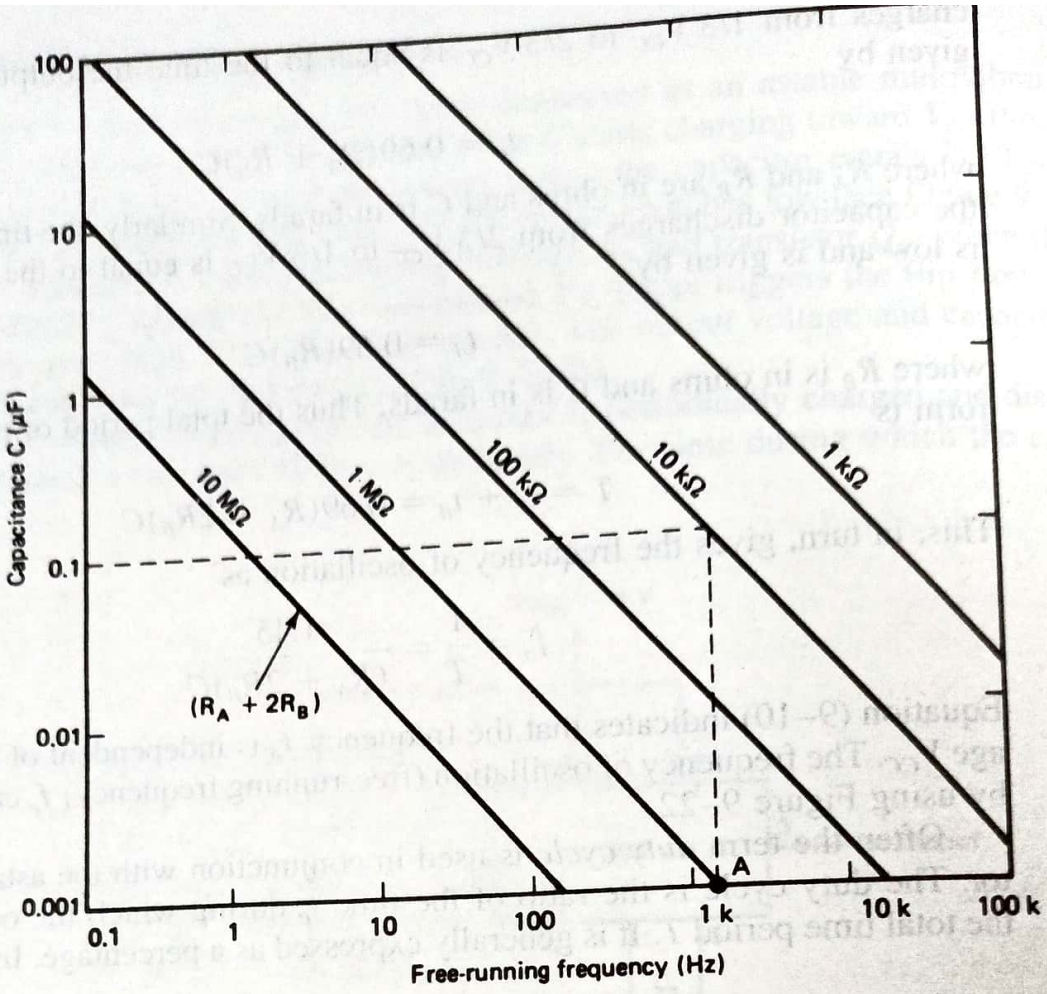


FIGURE 9–22 Free-running frequency versus R_A, R_B, and C.

SOLUTION

From Equations (9–8a) and (9–8b),

$$t_c = (0.69)(2.2\ \text{k}\Omega + 3.9\ \text{k}\Omega)(0.1)(10^{-6})$$
$$= 0.421\ \text{ms}$$
$$t_d = (0.69)(3.9\ \text{k}\Omega)(0.1)(10^{-6})$$
$$= 0.269\ \text{ms}$$

Therefore,

$$f_o = \frac{1}{(0.421 + 0.269)(10^{-3})} = 1.45\ \text{kHz}$$

Using $C = 0.1\ \mu\text{F}$ and $R_A = 2R_B = 10\ \text{k}\Omega$, the free-running frequency can also be found from the graph in Figure 9–22, as indicated by point *A*. Note that the graph uses the log-log scale; that is, vertical and horizontal axes are marked in logarithmic scales.

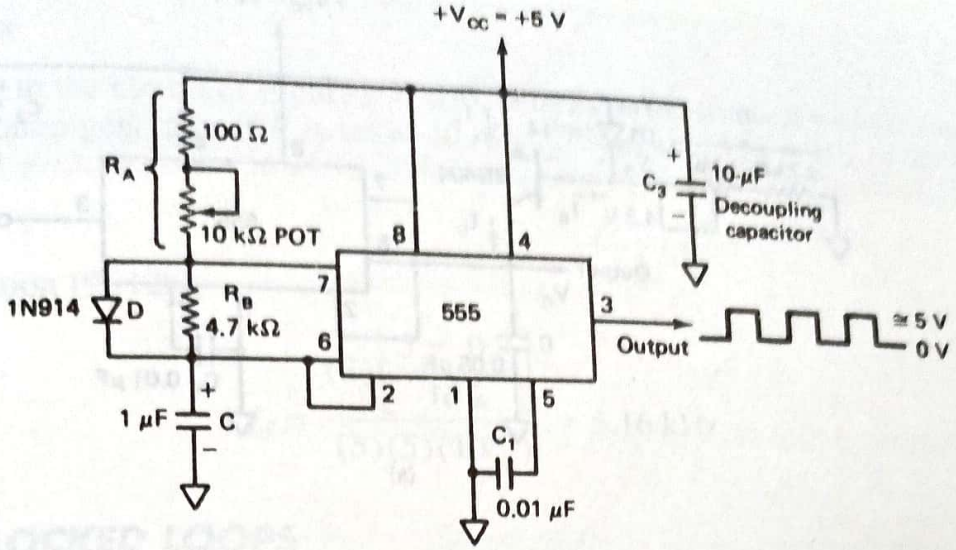


FIGURE 9–23 Astable multivibrator as a square wave oscillator.

9–4–4 Astable Multivibrator Applications

9–4–4(a) Square-wave oscillator

Without reducing $R_A = 0\ \Omega$, the astable multivibrator can be used to produce a square wave output simply by connecting diode D across resistor R_B, as shown in Figure 9–23. The capacitor C charges through R_A and diode D to approximately 2/3 V_{CC} and discharges through R_B and terminal 7 (transistor Q_1) until the capacitor voltage equals approximately 1/3 V_{CC}; then the cycle repeats. To obtain a square wave output (50% duty cycle), R_A must be a combination of a fixed resistor and potentiometer so that the potentiometer can be adjusted for the exact square wave.

9–4–4(b) Free-running ramp generator

The astable multivibrator can be used as a free-running ramp generator when resistors R_A and R_B are replaced by a current mirror. Figure 9–24(a) shows an astable multivibrator configured to perform this function. The current mirror starts charging capacitor C toward V_{CC} at a constant rate. When voltage across C equals 2/3 V_{CC}, comparator 1 turns transistor Q_1 on, and C rapidly discharges through transistor Q_1. Refer to Figure 9–15(b). However, when the discharge voltage across C is approximately equal to 1/3 V_{CC}, comparator 2 switches transistor Q_1 off, and then capacitor C starts charging up again. Thus the charge–discharge cycle keeps repeating. The discharging time of the capacitor is relatively negligible compared to its charging time; hence, for all practical purposes, the time period of the ramp waveform is equal to the charging time and is approximately given by

$$T = \frac{V_{CC}C}{3I_C} \qquad \textbf{(9–12a)}$$

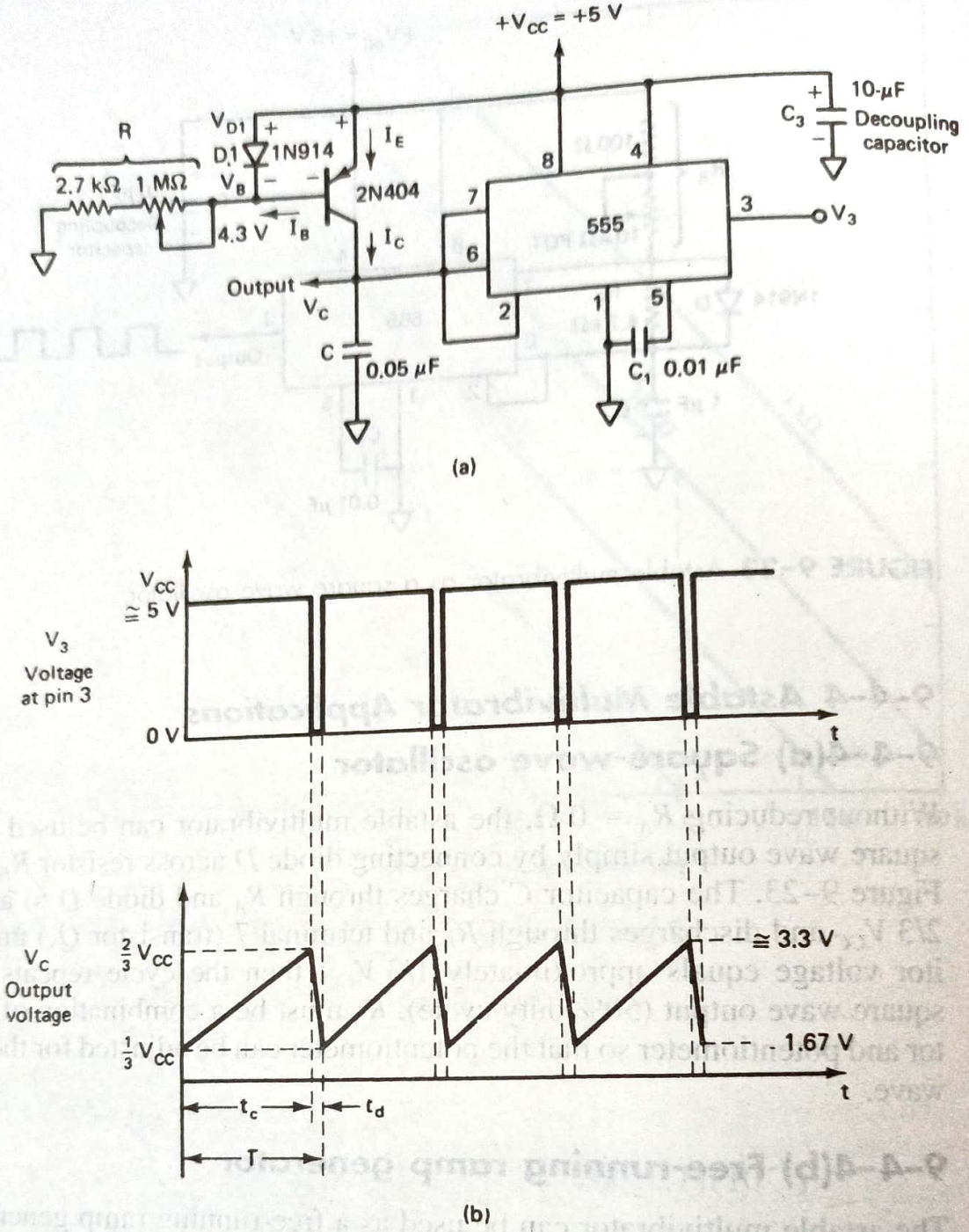


FIGURE 9–24 (a) Free-running ramp generator circuit. (b) Output waveform.

where $I_C = (V_{CC} - V_{BE})/R$ = constant current in amperes and C is in farads. Therefore, the free-running frequency of the ramp generator is

$$f_o = \frac{3I_C}{V_{CC}C} \qquad (9\text{–}12b)$$

Figure 9–24(b) shows the generator's output waveform.

EXAMPLE 9–8

Referring to the circuit of Figure 9–24(a), determine the frequency of the free-running ramp generator if R is set at 10 kΩ. Assume that $V_{BE} = V_{D1} = 0.7$ V.

SOLUTION

By Equation (9–12b),

$$f_o = \frac{(3)\left[\dfrac{5 - 0.7}{10\text{ k}}\right]}{(5)(5)(10^{-8})} = 5.16\text{ kHz}$$

9–5 PHASE-LOCKED LOOPS

Although the evolution of the phase-locked loop began in the early 1930s, its cost outweighed its advantages at first. With the rapid development of integrated-circuit technology, however, the phase-locked loop has emerged as one of the fundamental building blocks in electronics technology. The phase-locked loop principle has been used in applications such as FM (frequency modulation) stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM demodulators, frequency shift keying (FSK) decoders, and a generation of local oscillator frequencies in TV and in FM tuners. Today the phase-locked loop is even available as a single package, typical examples of which include the Signetics' SE/NE 560 series (the 560, 561, 562, 564, 565, and 567). However, for more economical operation, discrete ICs can be used to construct a phase-locked loop.

9–5–1 Operating Principles

Figure 9–25 shows the phase-locked loop (PLL) in its basic form. As illustrated in this figure, the phase-locked loop consists of (1) a phase detector, (2) a low-pass filter, and (3) a voltage-controlled oscillator.

The phase detector, or comparator compares the input frequency f_{IN} with the feedback frequency f_{OUT}. The output of the phase detector is proportional to the phase difference between f_{IN} and f_{OUT}. The output voltage of a phase detector is a dc voltage and therefore is often referred to as the *error* voltage. The output of the phase detector is then applied to the low-pass filter, which removes the high-frequency noise and produces a dc level. This dc level, in turn, is the input to the voltage-controlled oscillator (VCO). The filter also helps in establishing the dynamic characteristics of the PLL circuit. The output frequency of the VCO is directly proportional to the input dc level. The VCO frequency is compared with the input frequencies and adjusted until it is equal to the input frequencies. In short, the phase-locked loop goes through three states: *free-running*, *capture*, and *phase lock*.

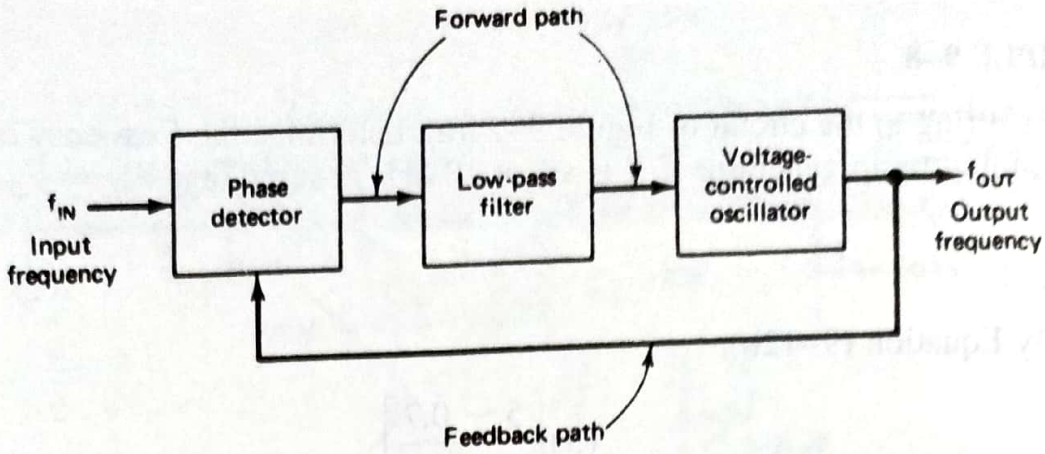


FIGURE 9–25 Block diagram of a phase-locked loop.

Before the input is applied, the phase-locked loop is in the free-running state. Once the input frequency is applied, the VCO frequency starts to change and the phase-locked loop is said to be in the capture mode. The VCO frequency continues to change until it equals the input frequency, and the phase-locked loop is then in the phase-locked state. When phase locked, the loop tracks any change in the input frequency through its repetitive action.

Before studying the specialized phase-locked-loop IC, we shall consider the discrete phase-locked loop, which may be assembled by combining a phase detector, a low-pass filter, and a voltage-controlled oscillator (see Figure 9–25).

9–5–1(a) Phase detector

The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies. Depending on whether the analog or digital phase detector is used, the PLL is called either an analog or digital type, respectively. Even though most of the monolithic PLL integrated circuits use analog phase detectors, the majority of discrete phase detectors in use are of the digital type mainly because of its simplicity. For this reason, we shall consider only digital-type phase detectors here.

A double-balanced mixer is a classic example of an analog phase detector. On the other hand, examples of digital phase detectors are these:

1. Exclusive-OR phase detector
2. Edge-triggered phase detector
3. Monolithic phase detector (such as type 4044)

Figure 9–26(a) shows the exclusive-OR phase detector that uses an exclusive-OR gate such as CMOS type 4070. The output of the exclusive-OR gate is *high* only when f_{IN} or f_{OUT} is high, as shown in Figure 9–26(b).

In this figure, f_{IN} is leading f_{OUT} by ϕ (phi) degrees; that is, the phase difference between f_{IN} and f_{OUT} is ϕ degrees. The dc output voltage of the exclusive-OR phase detector is a function of the phase difference between its two inputs.

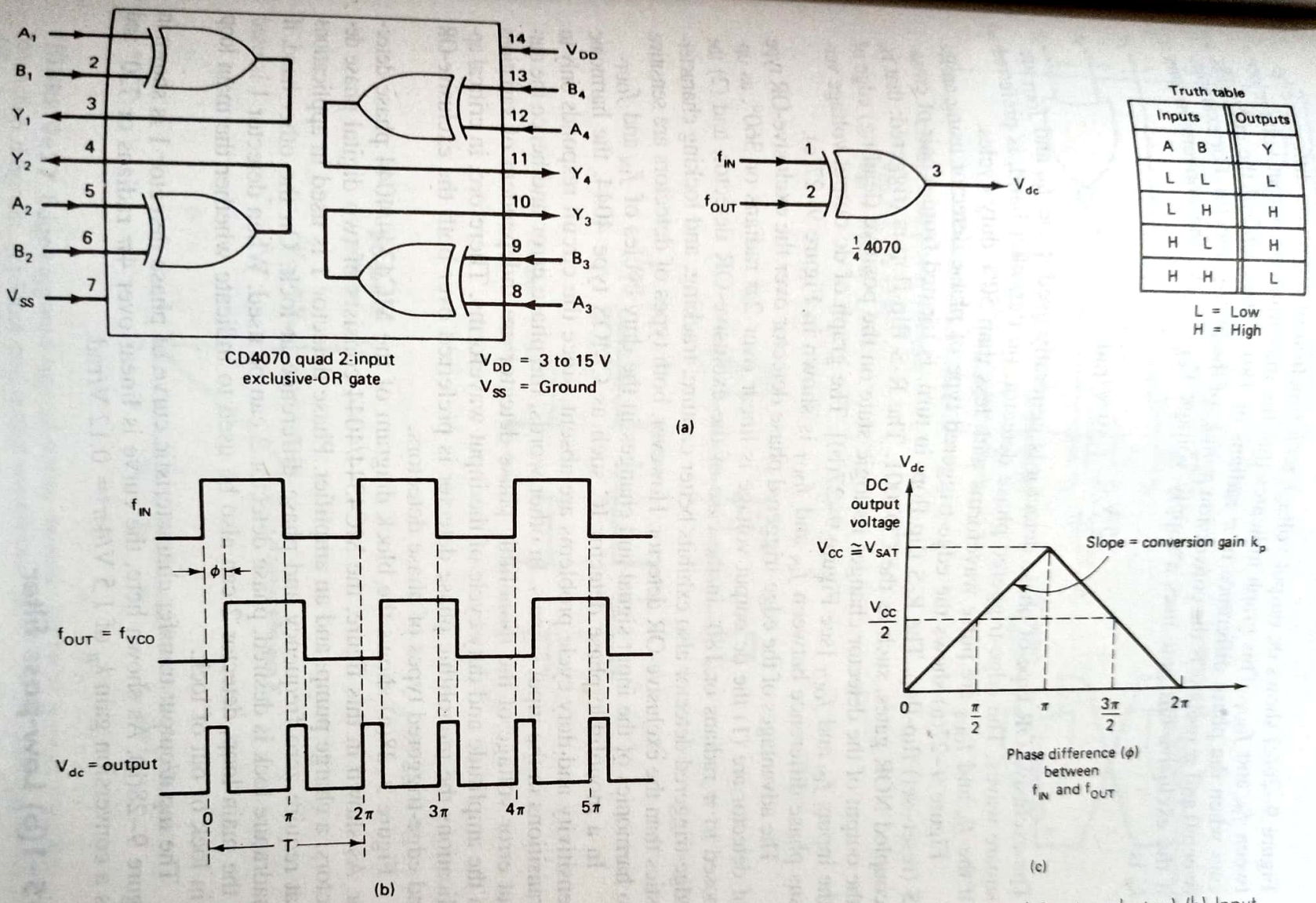


FIGURE 9–26 (a) Exclusive-OR phase detector connection and logic diagram. (Courtesy of National Semiconductor.) (b) Input and output waveforms. (c) Average output voltage versus phase difference between f_{IN} and f_{OUT} curve.

Figure 9–26(c) shows dc output voltage as a function of the phase difference between f_{IN} and f_{OUT}. This graph indicates that the maximum dc output voltage occurs when the phase difference is π radians or 180°. The slope of the curve between 0 and π radians is the conversion gain k_p of the phase detector. For example, if the exclusive-OR gate uses a supply voltage $V_{CC} = 5$ V, the conversion gain k_p is

$$k_p = \frac{5 \text{ V}}{\pi} = 1.59 \text{ V/rad}$$

The exclusive-OR type of phase detector is generally used if the f_{IN} and f_{OUT} are square waves. The edge-triggered phase detector, on the other hand, is preferred if the f_{IN} and f_{OUT} are pulse waveforms with less than 50% duty cycles.

Figure 9–27(a) shows the edge-triggered type of phase detector using an R-S (reset–set) flip-flop. The R-S flip-flop, in turn, is formed from a pair of cross-coupled NOR gates, such as the CD4001. The R-S flip-flop is triggered; that is, the output of the detector changes its logic state on the positive (leading) edge of the inputs f_{IN} and f_{OUT} [see Figure 9–27(b)]. The graph of dc output voltage versus phase difference between f_{IN} and f_{OUT} is shown in Figure 9–27(c).

The advantages of the edge-triggered phase detector over the exclusive-OR type of detector are (1) the dc output voltage is linear over 2π radians or 360°, as opposed to π radians or 180° in the case of the exclusive-OR detector, and (2) the edge-triggered detector also exhibits better capture, tracking, and locking characteristics than the exclusive-OR detector. However, both types of detectors are sensitive to harmonics of the input signal and changes in the duty cycles of f_{IN} and f_{OUT}.

In a monolithic phase detector IC such as CMOS type 4044, the harmonic sensitivity and duty cycle problems are absent, since the circuit responds only to transitions in the input signals. In other words, the phase error and hence the output error voltage of the monolithic phase detector are independent of variations in the amplitude and duty cycle of the input waveforms. Therefore, in critical applications the monolithic phase detector is preferred over both the exclusive-OR and edge-triggered types of phase detectors.

Figure 9–28(a) shows the block diagram of the MC4344/4044 phase detector. As shown in this figure, the MC4344/4044 consists of two digital phase detectors, a charge pump, and an amplifier. Phase detector 1 is used in applications that require zero frequency and phase difference at lock. On the other hand, if quadrature lock is desired, phase detector 2 can be used. When detector 1 is used in the main loop, detector 2 can also be used to indicate whether the main loop is in lock or out of lock.

The input/output transfer characteristic curve of phase detector 1 is shown in Figure 9–28(b). As shown here, the curve is linear over 4π radians or 720° and has a conversion gain k_p of 1.5 V/4π = 0.12 V/rad.

9–5–1(b) Low-pass filter

The second block shown in the PLL block diagram of Figure 9–25 is a low-pass filter. The function of the low-pass filter is to remove the high-frequency

igure 9–29(c) includes

9-5-1(c) Voltage-controlled oscillator

The third section of the PLL is the voltage-controlled oscillator. The VCO generates an output frequency that is directly proportional to its input voltage. The block diagram of the VCO is shown in Figure 9–30.

FIGURE 9–30 VCO block diagram.

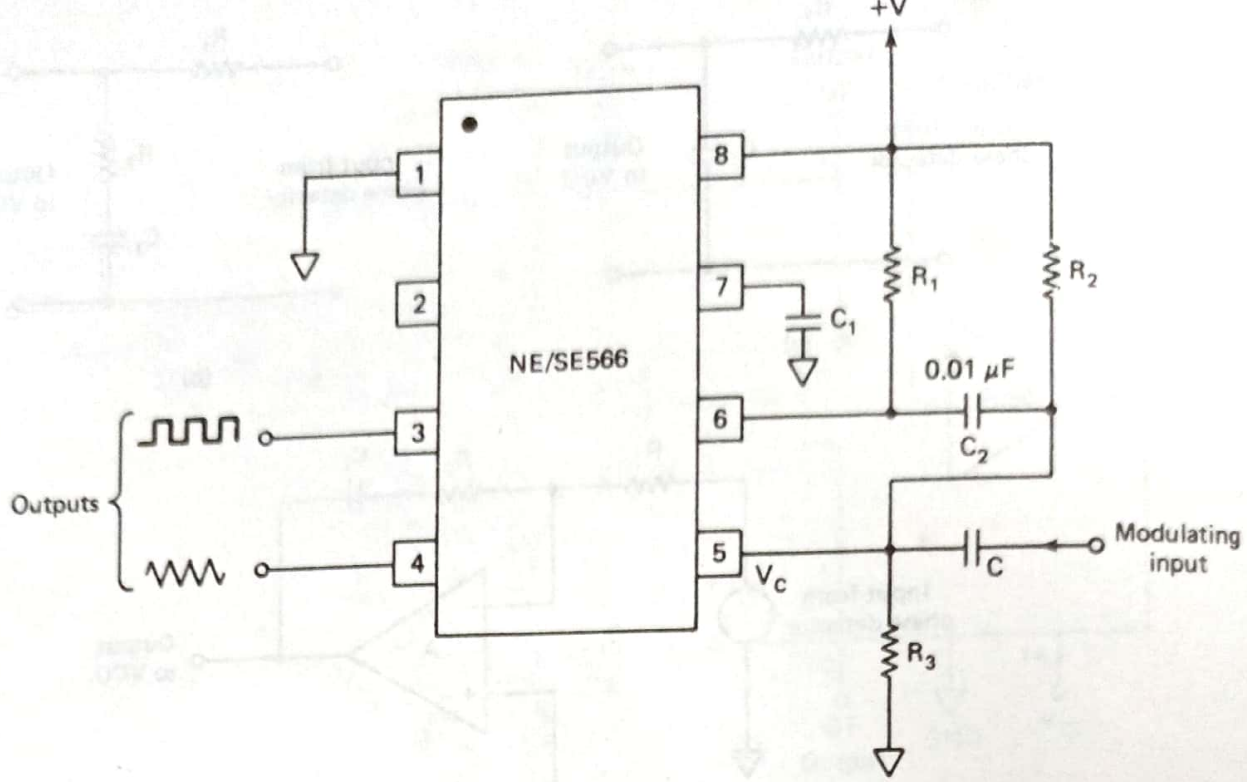


FIGURE 9–31 NE/SE566 VCO connection diagram.

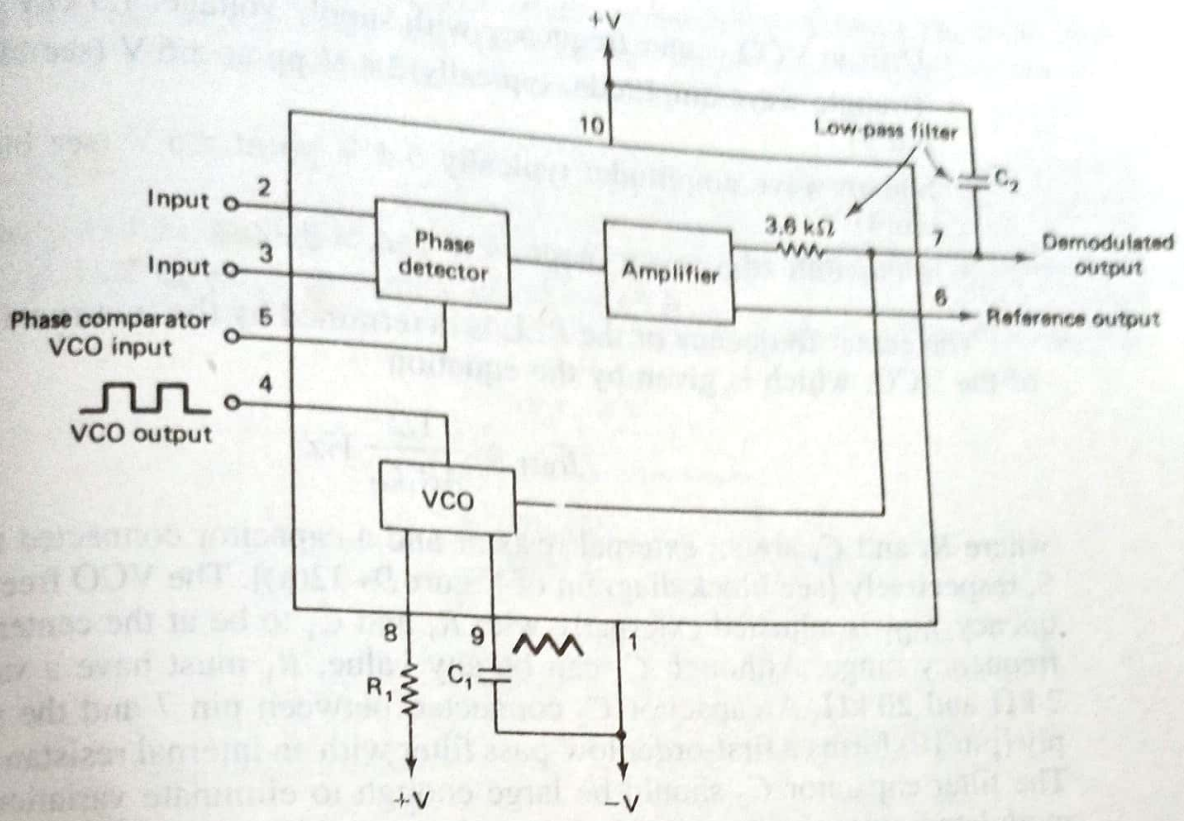
While the SE/NE 566 VCO is discussed in Section 7-18, a typical connection diagram is repeated in Figure 9–31, for convenience. The maximum output frequency of the NE/SE 566 is 500 kHz. For higher output frequency, therefore, integrated circuits such as Motorola's MC4324/4024 and MC1648 may be used.

9–5–2 Monolithic Phase-Locked Loops

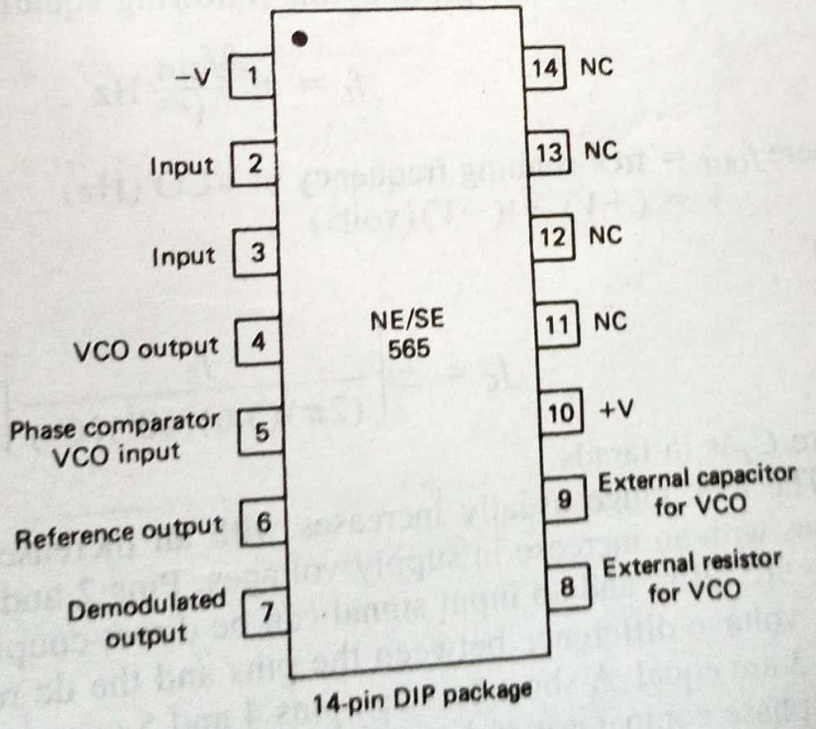
The Signetics SE/NE 560 series is monolithic phase-locked loops. The SE/NE 560, 561, 562, 564, 565, and 567 differ mainly in operating frequency range, power supply requirements, and frequency and bandwidth adjustment ranges. Only the SE/NE 565 phase-locked loop is discussed here because it is one of the most commonly used devices of the 560 series.

Figure 9–32 shows the block diagram and connection diagram of the 565 PLL. The device is available as a 14-pin DIP package and as a 10-pin metal can package. The important electrical characteristics of the 565 PLL are:

- Operating frequency range: 0.001 Hz to 500 kHz
- Operating voltage range: ±6 to ±12 V
- Input level required for tracking: 10 mV rms minimum to 3 V peak-to-peak maximum
- Input impedance: 10 kΩ typically
- Output sink current: 1 mA, typically
- Output source current: 10 mA, typically
- Drift in VCO center frequency (f_{OUT}) with temperature: 300 ppm/°C, typically



(a)



(b)

FIGURE 9–32 (a) NE/SE565 PLL block diagram. (b) Connection diagram. (Courtesy of Signetics Corporation.)

- Drift in VCO center frequency with supply voltage: 1.5%/V maximum
- Triangle wave amplitude: typically 2.4 V pp at ±6 V (see block diagram, pin 9)
- Square wave amplitude: typically 5.4 V pp at ±6 V (see block diagram, pin 4)
- Bandwidth adjustment range: $< \pm 1$ to $> \pm 60\%$

The center frequency of the PLL is determined by the free-running frequency of the VCO, which is given by the equation

$$f_{OUT} \cong \frac{1.2}{4R_1C_1} \text{ Hz} \tag{9–13}$$

where R_1 and C_1 are an external resistor and a capacitor connected to pins 8 and 9, respectively [see block diagram of Figure 9–32(a)]. The VCO free-running frequency f_{OUT} is adjusted externally with R_1 and C_1 to be at the center of the input frequency range. Although C_1 can be any value, R_1 must have a value between 2 kΩ and 20 kΩ. A capacitor C_2 connected between pin 7 and the positive supply (pin 10) forms a first-order low-pass filter with an internal resistance of 3.6 kΩ. The filter capacitor C_2 should be large enough to eliminate variations in the demodulated output voltage at pin 7 in order to stabilize the VCO frequency.

The 565 PLL can lock to and track an input signal over typically ±60% bandwidth with respect to f_{OUT} as the center frequency. The lock range f_L and capture range f_C of the PLL are given by the following equations:

$$f_L = \pm \frac{8f_{OUT}}{V} \text{ Hz} \tag{9–14}$$

where f_{OUT} = free-running frequency of VCO (Hz)
$V = (+V) - (-V)$ (volts)

and

$$f_C = \pm \left[\frac{f_L}{(2\pi)(3.6)(10^3)(C_2)} \right]^{1/2} \tag{9–15}$$

where C_2 is in farads.

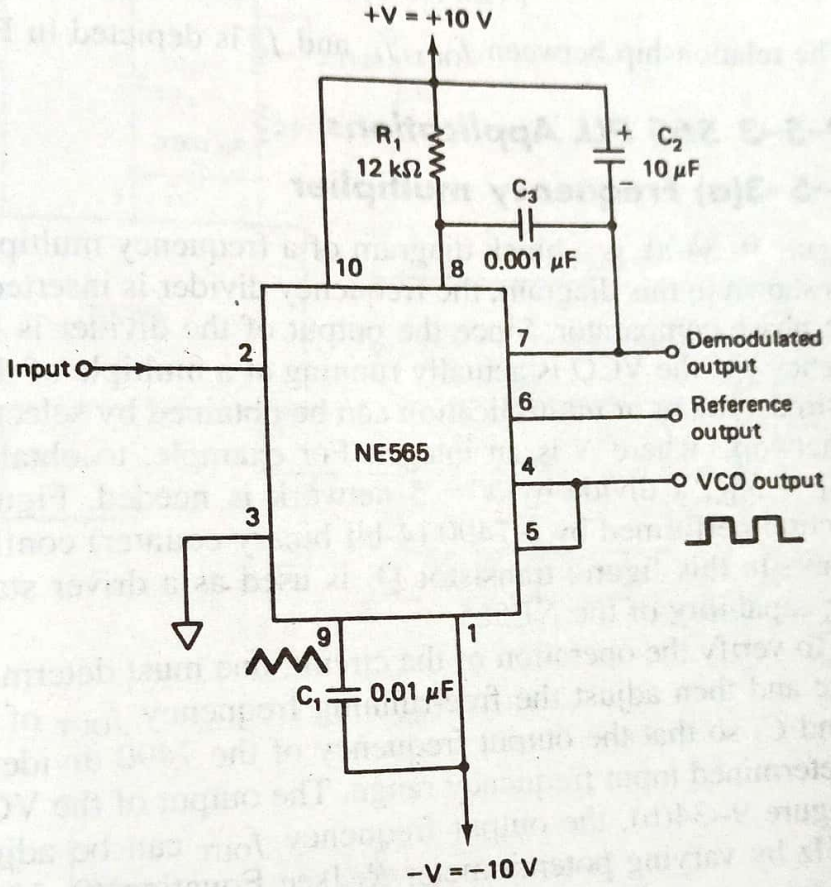
The lock range usually increases with an increase in input voltage but decreases with an increase in supply voltages. Pins 2 and 3 are the input terminals of the 565 PLL, and an input signal can be direct-coupled, provided that there is no dc voltage difference between the pins and the dc resistances seen from pins 2 and 3 are equal. A short between pins 4 and 5 connects the VCO output (f_{OUT}) to the phase comparator and enables the comparator to compare f_{OUT} with the input signal f_{IN}.

In frequency multiplication applications a digital frequency divider is inserted between pins 4 and 5, as will be shown later. A dc reference voltage at pin 6 is approximately equal to the dc potential of the demodulated output at pin 7. In applications such as frequency shift keying (FSK), the dc reference voltage at pin 6

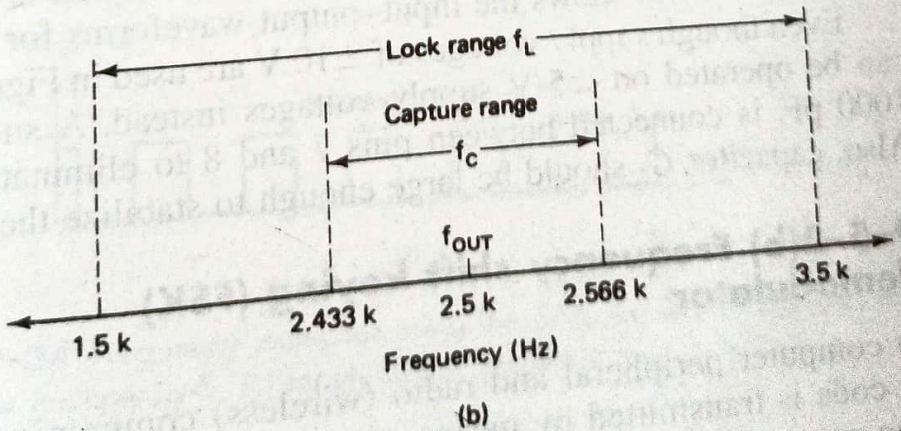
is used as an input to the comparator. [Refer to Section 9–5.3(b).] The lock range of the PLL can be decreased with little change in the free-running frequency of the VCO by connecting a resistance between pins 6 and 7.

EXAMPLE 9–9

Referring to the circuit of Figure 9–33(a), determine the free-running frequency f_{OUT}, the lock range f_L, and the capture range f_C.



(a)



(b)

FIGURE 9–33 (a) Circuit of Example 9–9. (b) Relationship between f_{OUT}, f_L, and f_C.

SOLUTION

From Equations (9–13) through (9–15),

$$f_{OUT} = \frac{1.2}{(4)(12)(10^3)(10^{-8})} = 2.5 \text{ kHz}$$

$$f_L = \pm\frac{8(2.5)(10^3)}{(20)} = \pm 1 \text{ kHz}$$

$$f_C = \pm\left[\frac{(10^3)}{(2\pi)(3.6)(10^3)(10)(10^{-6})}\right]^{1/2} = \pm 66.49 \text{ Hz}$$

The relationship between f_{OUT}, f_L, and f_C is depicted in Figure 9–33(b).