D/A and A/D Converters (DAC and ADC)

By:- ABose

Digital to Analog converters (DAC)

A device which produces an analog output voltage from a given digital input is called digital-to-analog (D/A) converters. Ex:- printers, plotters etc.

Two types of DAC can be described by using OP AMP.

i) The weighted resistor D/A converters:

Let us consider a conversion of a 4-bit digital word into an analog form.

The decimal equivalent (N) of a 4-bit digital word $B_3B_2B_1B_0$ is,

$$N = 2^3B_3 + 2^2B_2 + 2^1B_1 + 2^0B_0$$ ($B_i = 0$ or 1 and B_i is bit)

B_0 = LSB and B_3 = MSB.

The basic circuit for this conversion of a 4-bit word using an OP AMP is shown in figure below. (Fig-1)

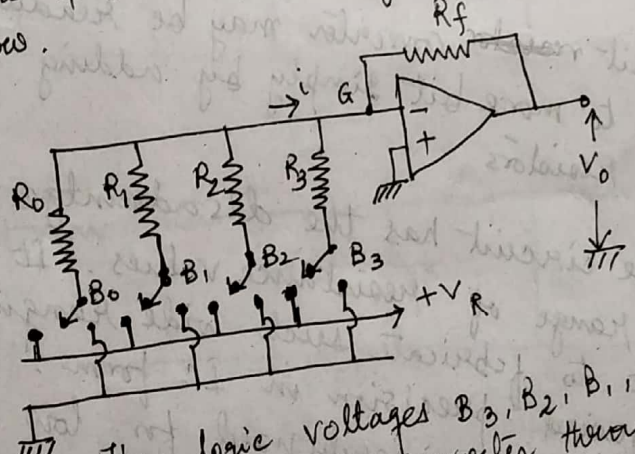

Fig-1

The logic voltages B_3, B_2, B_1, B_0 are applied to the resistors of the converter through switches. When the coefficient B_i is 1, the switch is closed, thus connecting stabilized voltage source V_R to the converter; when B_i is 0, the corresponding switch is connected to the ground. The resistors R_0, R_1, R_2 and R_3 in the circuit are weighted.

so that the successive resistors ratio is 2.

i.e, $\frac{R_0}{R_1} = \frac{R_1}{R_2} = \frac{R_2}{R_3} = 2$ and each resistor is inversely proportional to the numerical significance of the appropriate binary bit.

Thus, if R is the arbitrary resistance selected to suit impedance level of the ckt circuit, then

$$R_0 = \frac{R}{2^0} = R, \quad R_1 = \frac{R}{2^1} = \frac{R}{2}, \quad R_2 = \frac{R}{2^2} = \frac{R}{4} \text{ and}$$

$$R_3 = \frac{R}{2^3} = \frac{R}{8}.$$

The current i to the inv. input terminal is

$$i = V_R\left(\frac{B_3}{R_3} + \frac{B_2}{R_2} + \frac{B_1}{R_1} + \frac{B_0}{R_0}\right)$$

$$= \frac{V_R}{R}\left(2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0\right)$$

Since G is virtual ground, output voltage,

$$V_0 = -iR_f = -\frac{V_R}{R} R_f \left(2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0\right)$$

Thus the output voltage is proportional to the numerical value of the binary input.

4-bit converter may be readily extended to more bit simply by adding more weighted resistors

The circuit has the disadvantge of using wide range of resistance values. It is difficult to fabricate such wide ranging resistance with required precision in IC form. For this, this circuit is primarily used for low resolution applications.

ii) The R-2R Ladder Converter (D/A):

The resistive ladder converter for a 4-bit digital word is shown in figure below (Fig 2)

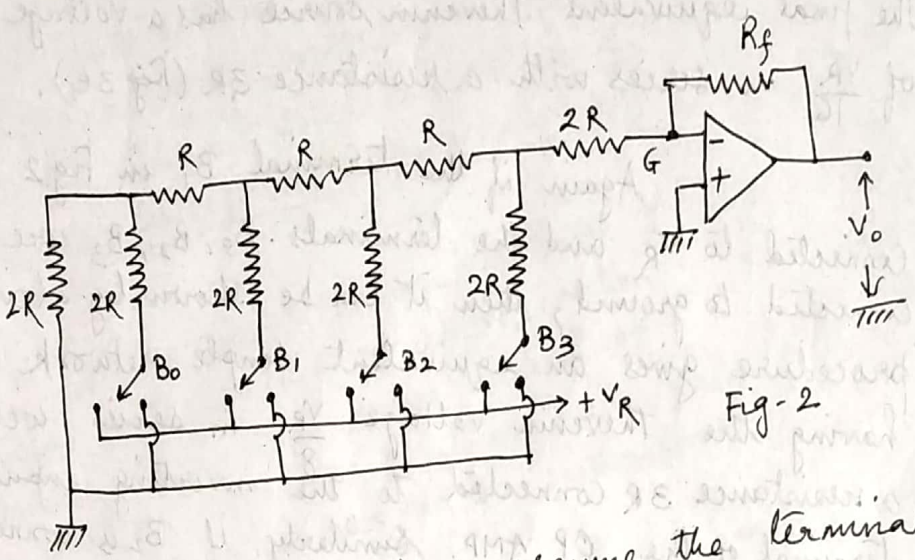

Fig-2

To explain the operation, assume the terminal B_0 is connected to V_R and all other terminals namely, B_1, B_2 and B_3 are connected to ground. The resulting resistive portion of the ladder is shown in figure (Fig-3a).

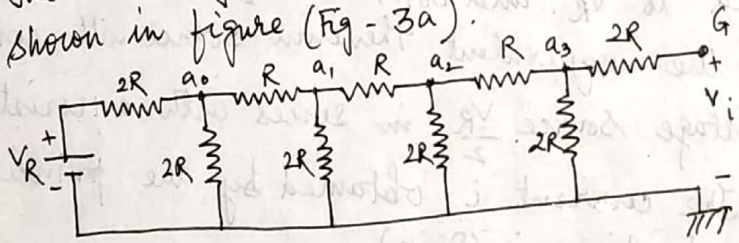

Fig 3a.

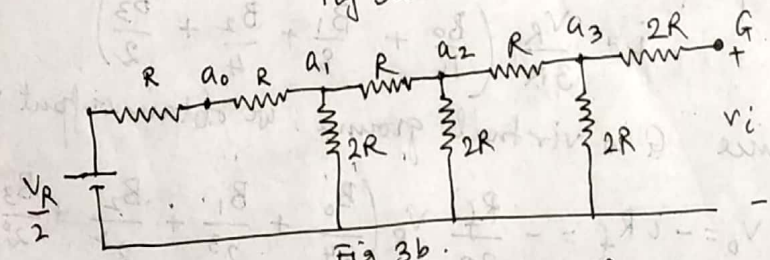

Fig 3b.

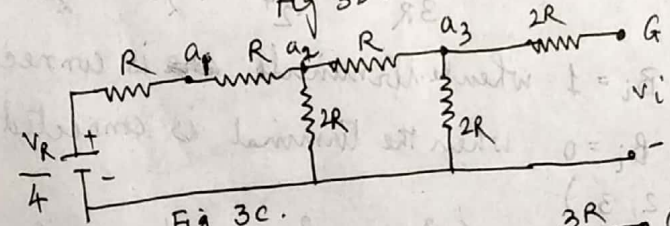

Fig 3c.

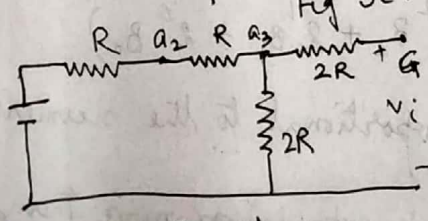

Fig 3d

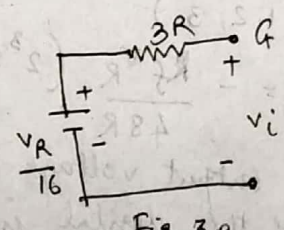

Fig 3e

Fig 3: Thevenin Equivalent circuit

Applying Thevenin's theorem successively to the nodes a_0, a_1, a_2 and a_3, with respect to ground we obtain equivalent Thevenin's network shown in Fig 3a, 3b, 3c, 3d and 3e respectively. The final equivalent Thevenin source has a voltage of $\frac{V_R}{16}$ in series with a resistance 3R (Fig 3e).

Again if the terminal B_1 in Fig 2 is connected to V_R and the terminals B_0, B_2, B_3 are connected to ground, then it can be shown by above procedure gives an equivalent simple network having the Thevenin voltage $\frac{V_R}{8}$ in series with a resistance 3R connected to the inverting input terminal of the OP AMP. Similarly, if B_2 is connected to V_R, and B_0, B_1 and B_3 are grounded, the corresponding Thevenin equivalent has a voltage $\frac{V_R}{4}$ with a resistance 3R in series. Lastly, when the terminal B_3 is connected to V_R, and B_0, B_1 and B_2 are connected to ground, the equivalent Thevenin source will consist of a voltage source $\frac{V_R}{2}$ in series with a resistance 3R.

The current i obtained by the principle of superposition is (Fig 2)

$$i = \frac{V_R}{3R}\left(\frac{B_0}{16} + \frac{B_1}{8} + \frac{B_2}{4} + \frac{B_3}{2}\right)$$

Since G is virtual ground. we obtain output voltage,

$$V_0 = -iR_f = -\frac{R_f}{3R} V_R \left(\frac{B_0}{2^4} + \frac{B_1}{2^3} + \frac{B_2}{2^2} + \frac{B_3}{2^0}\right)$$

Here, $B_i = 1$ when the terminals is connected to V_R and $B_i = 0$ when the terminal is connected to ground $(i = 0, 1, 2, 3)$

$$\therefore V_0 = -\frac{R_f V_R}{48R}\left(2^3 B_3 + 2^2 B_2 + 2^1 B_1 + 2^0 B_0\right)$$

The output voltage is proportional to the numerical value of the digital input.

The above circuit can be extended for more than 4 bits by incorporating additional switches and sections to the ladder.

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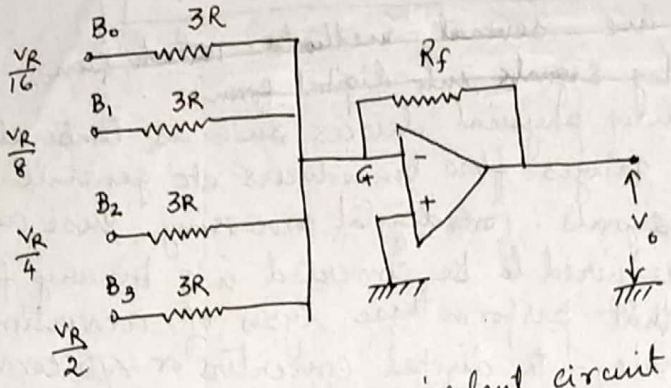

Fig 4: Final equivalent circuit.

In a 4-bit converter the smallest change in the output voltage (due to change of one unit at the input) i,e, resolution of the converter is given by.

$$\frac{\text{Full scale voltage}}{\text{Number of steps}} = \frac{R_f}{3R}\frac{V_R}{2^4} = V_R \frac{R_f}{48R}$$

With $V_R = 5V$ and $R_f = 3R$, voltage resolution is of the order 0.3V. In a 4-bit D/A converter the input binary word varies from 0000 to 1111 (0 to 15) and the output of the converter could assume a staircase waveform with $2^4 - 1$ or 15 discrete steps (Fig 5).

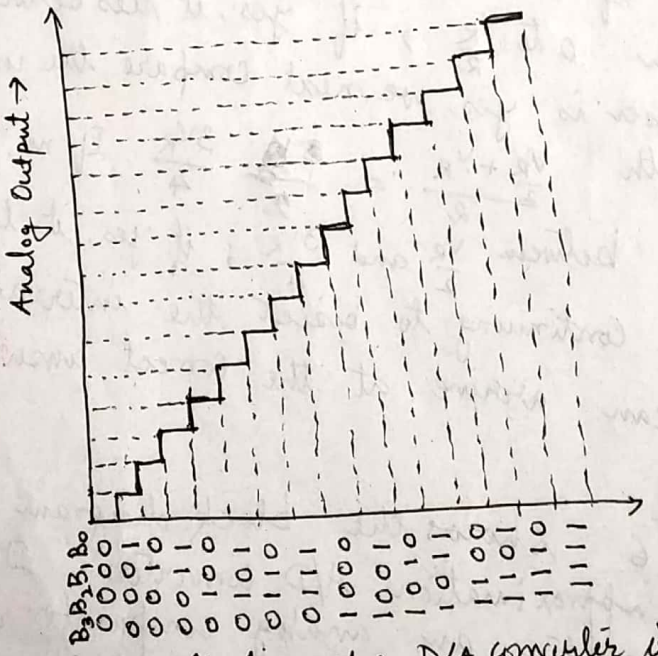

Fig 5 :- Input Output conversion graph.

Another specification of a D/A converter is accuracy of conversion. It is a measure of the difference between the actual analog output voltage and the expected output voltage. Practically the accuracy of converter should be no worse than $\pm\frac{1}{2}$ LSB.

Analog-to-Digital Converter (ADC)

A large number of physical devices such as temperature and pressure gauges, flow transducers etc generate analog output signals. For digital processing, these analog outputs are required to be converted into binary form. The circuits that perform these types of conversions are called analog-to digital converters or A/D converters.

There are several such converters, of those, we will discuss <u>Successive approximation A/D converter</u>.

One of the most common method of A/D conversion is the successive approximation method. It uses trial and error method of numerical analysis and is a relatively faster method. The basic principle of working can be understood from the following example:

Suppose we want to measure a voltage in the range 0 to V_R. We begin with a comparator and ask the question "Is the unknown voltage is greater than $\frac{V_R}{2}$?" If the answer is no, the unknown voltage lies between 0 to $\frac{V_R}{2}$, if yes, it lies between $\frac{V_R}{2}$ and V_R. If the answer is yes, we next compare the unknown voltage with $\frac{V_R + V_R}{2}$ or $\frac{3V_R}{4}$. If no, the unknown voltage lies between $\frac{V_R}{2}$ and $\frac{3V_R}{4}$; if yes, it lies between $\frac{3V_R}{4}$ and V_R. Continuing to bisect the interval in this way, we can arrive at the correct answer very quickly.

Figure 6 shows the block diagram of a successive approximation A/D converter. It consists of a D/A converter, an analog comparator and a successive approximation register (SAR). To start the

the conversion, the SAR sets the MSB to 1 and all other bits to 0. This makes the output V_d of the D/A converter to be $\frac{V_R}{2}$. The comparator compare it with the analog input voltage V_a.

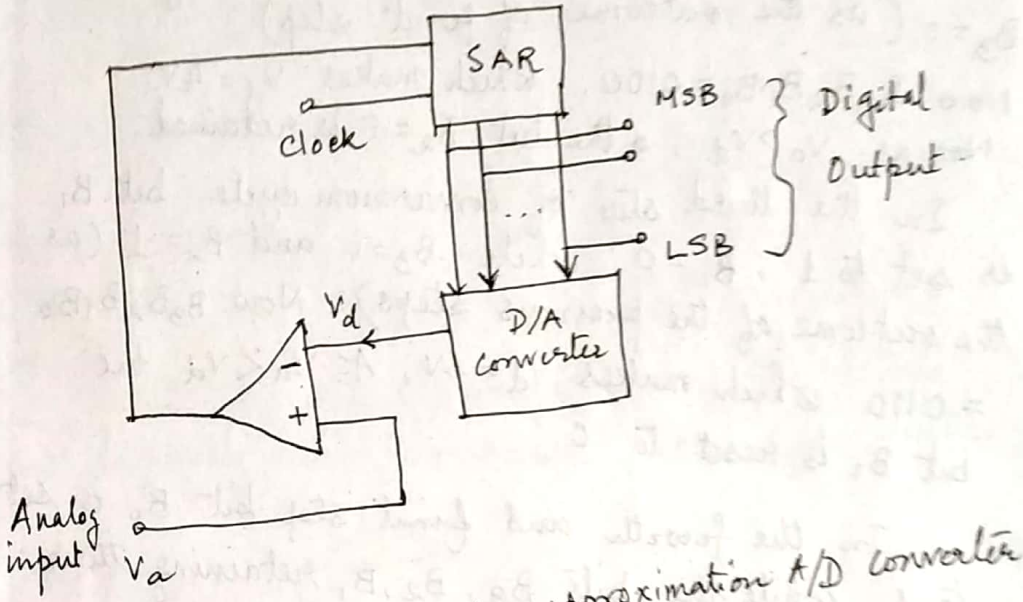

Fig 6: Successive approximation A/D converter

If $V_a > V_d \left(= \frac{V_R}{2}\right)$ the output of the comparator is high which keeps the MSB at 1. If $V_a < V_d \left(= \frac{V_R}{2}\right)$ the output of the comparator is low which resets the MSB to 0. The system does this with the MSB first, then the next significant bit, then the next and so on. Thus a 1 is tried in each bit of the D/A converter until at the end of the process, the binary equivalent of the analog input voltage is obtained. For an N-bit converter the number of clock pulse required would be N and is thus faster than the counter controlled A/D converter which requires 2^N pulses.

In order to understand the operation of this A/D converter, a 4-bit converter and an unknown voltage $V_a = 5V$ is considered. In the first step the MSB is set to 1 and all other bits are 0.

So the binary code in the register is $B_3B_2B_1B_0 = 1000$. The output of the D/A convorter $V_d = 8V$. Now as $V_a < V_d$ - MSB, B_3 is reset to 0.

In the second step of the conversion cycle, bit B_2 is set to 1, while B_1, B_0, remaining 0; $B_3 = 0$ (as the outcome of first step).

Now $B_3B_2B_1B_0 = 0100$ which makes $V_d = 4V$.

Now as $V_a > V_d$, the bit $B_2 = 1$ is retained.

In the third step of conversion cycle, bit B_1 is set to 1, $B_0 = 0$ while $B_3 = 0$ and $B_2 = 1$ (as the outcome of the previous steps). Now $B_3B_2B_1B_0 = 0110$ which makes $V_d = 6V$, As $V_a < V_d$ the bit B_1 is reset to 0.

In the fourth and final step bit B_0 is set to 1, while the bits B_3, B_2, B_1 retaining their earlier states. Therefore, now $B_3B_2B_1B_0 = 0101$ which corresponds to $V_d = 5V$.

All the 4 bits have been tried, thus completing the conversion cycle. At this point, the binary code of the register is 0101 which corresponds to the value 5V of the analog input voltage.

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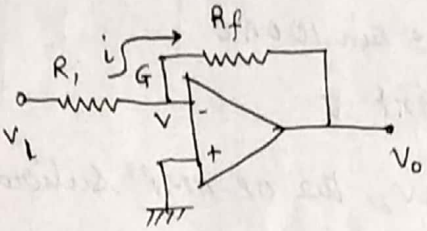
Problems (OP AMP)

Prob 1: In the inverting amplifier circuit, $R_1 = 1K\Omega$, and $R_f = 3K\Omega$. Determine the output voltage, the input resistance and the input current for an input voltage of 2V.



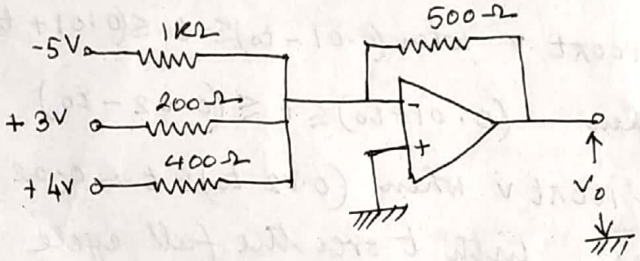
Soln: The output voltage is,

$$V_0 = -(R_f/R_1)V_1 = -(3/1) \times 2 = 6V$$ (Ans)

The input resistance $R_{in} = R_1 = 1K\Omega$

The input current, $i = \frac{V_1}{R_1} = \frac{2}{1} mA = 2mA$.

Prob 2: Find the output voltage V_0 of the three input summing amplifier circuit as in figure below.



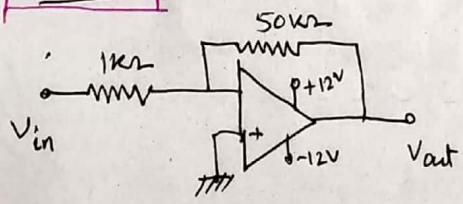
Soln: The output voltage should be,

$$V_0 = -\left[\frac{500}{1000} \times (-5) + \frac{500}{200} \times 3 + \frac{500}{400} \times 4\right]$$

$$= -(-2.5 + 7.5 + 5) = 10V.$$

$$\therefore \boxed{V_0 = 10V} \quad \text{(Ans)}.$$

Prob 3: Consider the OP AMP circuit as in figure below with a supply voltage of $\pm 12V$. Compute the gain and find the output if the input is given as, $V_{in} = 0.5 \sin 100\pi t$ volt.



Soln: Voltage gain of the given inverting amplifier is,

$$A = -\frac{50K\Omega}{1K\Omega} = -50$$

If the OP AMP were within linear region over the whole range of input, then the output voltage is,

$$V_{out} = AV_{in} = -50 \times 0.5 \sin 100\pi t$$
$$= -25 \sin 100\pi t \ V$$

Since the supply voltage is ±12V, the OP AMP saturates when V_{out} reaches 12V

Let at time $t = t_0$, $V_{out} = -12V$, Then

$$-12 = -25 \sin 100\pi t_0$$
$$\therefore t_0 = \frac{1}{100\pi} \sin^{-1}\left(\frac{12}{25}\right) = 1.59 \times 10^{-3} \text{ s.}$$

Thus, over the entire cycle we have

$V_{out} = -25 \sin 100\pi t \ V$ when $0 \le t \le t_0$

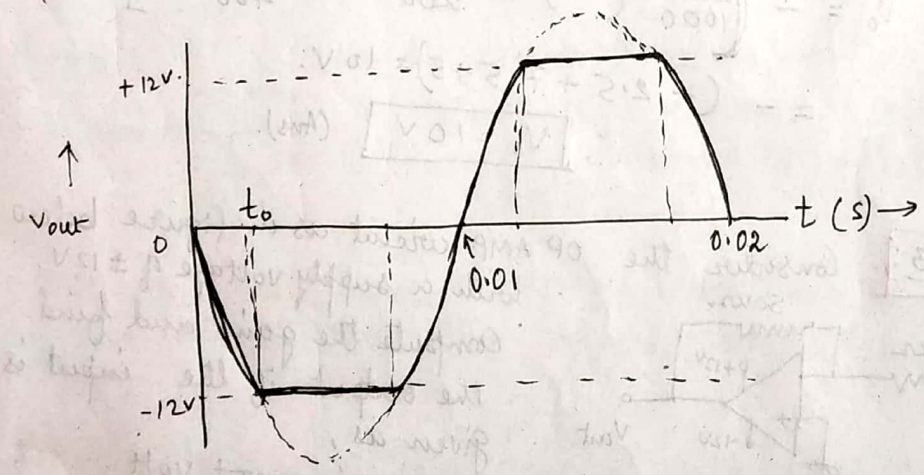
$= -12V$ when $t_0 \le t \le (0.01 - t_0)$

$= -25 \sin 100\pi t \ V$ when $(0.01 - t_0) \le t \le (0.01 + t_0)$

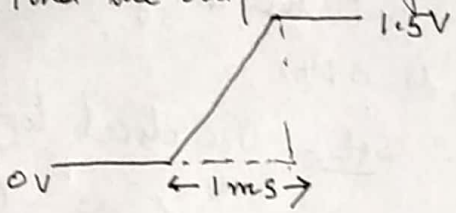
$= +12V$ when $(0.01 + t_0) \le t \le (0.02 - t_0)$

$= -25 \sin 100\pi t \ V$ when $(0.02 - t_0) \le t \le 0.02$ s.

The variation of V_{out} with t over the full cycle ($0 \le t \le 0.02$ s) is shown in figure below.



Prob 4: A ramp voltage of 1.5 V (as shown in fig) per millisecond is applied to an OP AMP differentiator having $R = 2\,k\Omega$ and $C = 0.01\,\mu F$. Find the output voltage and its waveform.



Input voltage, V_i

Soln:

The output voltage is

$$V_o = -RC \frac{dv_i}{dt}$$

Here v_i is shown in figure

For $0 < t < 1$ ms, $\frac{dv_i}{dt} = \frac{1.5V}{1ms}$

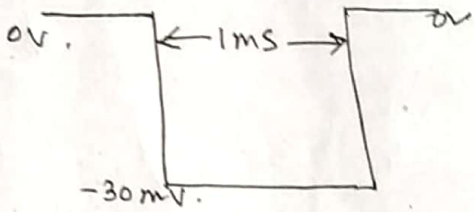
otherwise, $\frac{dv_i}{dt} = 0$.

Also, $RC = 2 \times 0.01 = 0.02$ ms.

Hence, $V_0 = -0.02 \times 1.5$ V

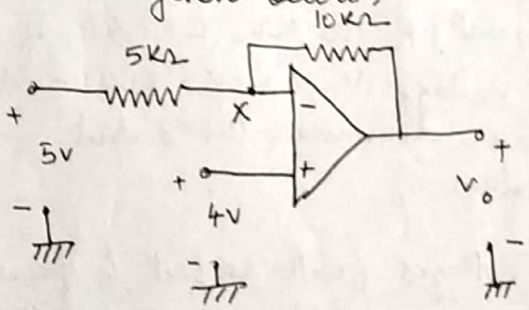
$= -0.03$ V $= -30$ mV for $0 < t < 1$ ms

$V_0 = 0$ otherwise



Output voltage, V_o

Prob 5: Calculate V_o of the circuit given below.



Soln: The gain of the OP AMP being infinite, the potential at the point X in the circuit is 4V. Applying Kirchhoff's current law at X, we obtain

$$\frac{V_0 - 4}{10\,K\Omega} = \frac{4-5}{5K\Omega} \Rightarrow V_o = 2V$$

(since input impedance of the OP AMP is infinite)

Prob 6: Find the bandwidth of the inverting OP AMP of $R_1 = 1K\Omega$ and $R_2 = 30K\Omega$, Assume that the unity gain bandwidth of the OP AMP is 3 MHz

Soln:- The closed loop gain of inverting OP AMP is

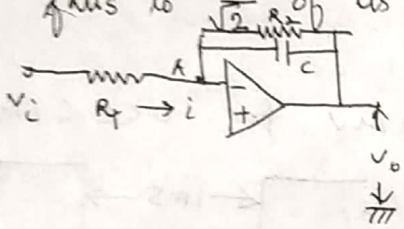
$$A_{vf} = -\frac{R_2}{R_1} = -30$$

Now, $|A_{vf}| \times$ bandwidth = Unity gain bandwidth

$\therefore$ The required bandwidth $= \frac{3\,MHz}{30}$

$= 100\,KHz$.

Prob 7: Show that in the practical OP AMP integrator circuit below, the frequency at which the voltage gain falls to $\frac{1}{\sqrt{2}}$ of its low frequency value is given by $1/2\pi CR_2$



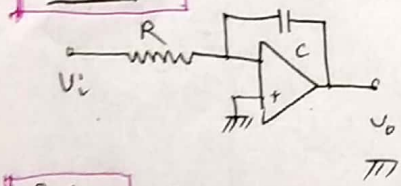
Soln: $\frac{V_o}{V_i} = \frac{R_2 \times \frac{1}{j\omega C}}{R_1\left(R_2 + \frac{1}{j\omega C}\right)} = \frac{R_2/R_1}{1 + j\omega C R_2}$

For $\omega = 0$, $\left|\frac{V_o}{V_i}\right| = \frac{R_2}{R_1}$ and

for $\omega C R_2 = 1$, $\left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{2}}\frac{R_2}{R_1}$

$\therefore$ The required frequency, $f = \frac{\omega}{2\pi} = 1/2\pi C R_2$

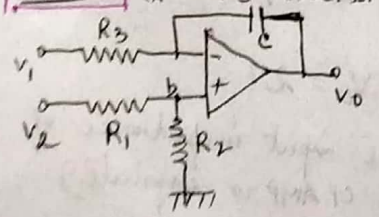
Prob 8:



In this circuit $R = 100\,K\Omega$, $C = 1\,\mu F$. If the input voltage V_i is $\pm 10V$, 250 Hz square wave, determine the output voltage V_o.

Prob 9: If V_1 and V_2 are two voltages (with respect to ground), how would you construct an OP AMP circuit to get the voltage $V_o = 2V_1 - V_2$?

Prob 10: In the circuit below, express V_o in terms of V_1 and V_2



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