INTRODUCTION TO COUNTERS

- *Flip-flops* are synchronous bi-stable devices. The term synchronous means the output changes state only when the clock input is triggered. That is, changes in the output occur in synchronization with the clock.
- An edge-triggered flip-flop changes states either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input.
- A counter is an application of flip-flop i.e. a sequential machine that produces a specified count sequence. The count changes whenever the input clock is asserted.
- There is a great variety of counter based on its construction.
    1. Clock: Synchronous or Asynchronous
    2. Clock Trigger: Positive edged or Negative edged
    3. Counts: Binary, Decade
    4. Count Direction: Up, Down, or Up/Down

INTRODUCTION TO COUNTERS

- A counter may count up or count down depending on the input control.
- For an n-bit counter, the range of the count is [0 to 2^{n-1}]. The count sequence usually repeats itself, unless designed otherwise [for "MOD-N and only N" counter, count sequence will go upto N after that the output will not change even after applying clocks]. When counting up, the count sequence goes in this manner: 0, 1, 2, … 2^{n-2}, 2^{n-1}, 0, 1, …etc. When counting down the count sequence goes in the same manner: 2^{n-1}, 2^{n-2}, … 2, 1, 0, 2^{n-1}, 2^{n-2}, … etc.
- **Asynchronous Counters (or Ripple counters)**:
    - The clock signal (CLK) is only used to clock the first FF.
    - Each FF (except the first FF) is clocked by the preceding FF.
- **Synchronous Counters**:
    - The clock signal (CLK) is applied to all FF, which means that all FF shares the same clock signal

INTRODUCTION TO COUNTERS

- An asynchronous counter circuit may behave as up or down counter depending on the input control and output terminal. Following table will illustrate it:

	Negative Edge Triggered clock pulse		Positive Edge Triggered clock pulse	
	Q to Clock i/p	$\overline{Q}$ to Clock i/p	Q to Clock i/p	$\overline{Q}$ to Clock i/p
Output Terminal	$\overline{Q}$ → down counter	$\overline{Q}$ → up counter	$\overline{Q}$ → up counter	$\overline{Q}$ → down counter
	Q → up counter	Q → down counter	Q → down counter	Q → up counter

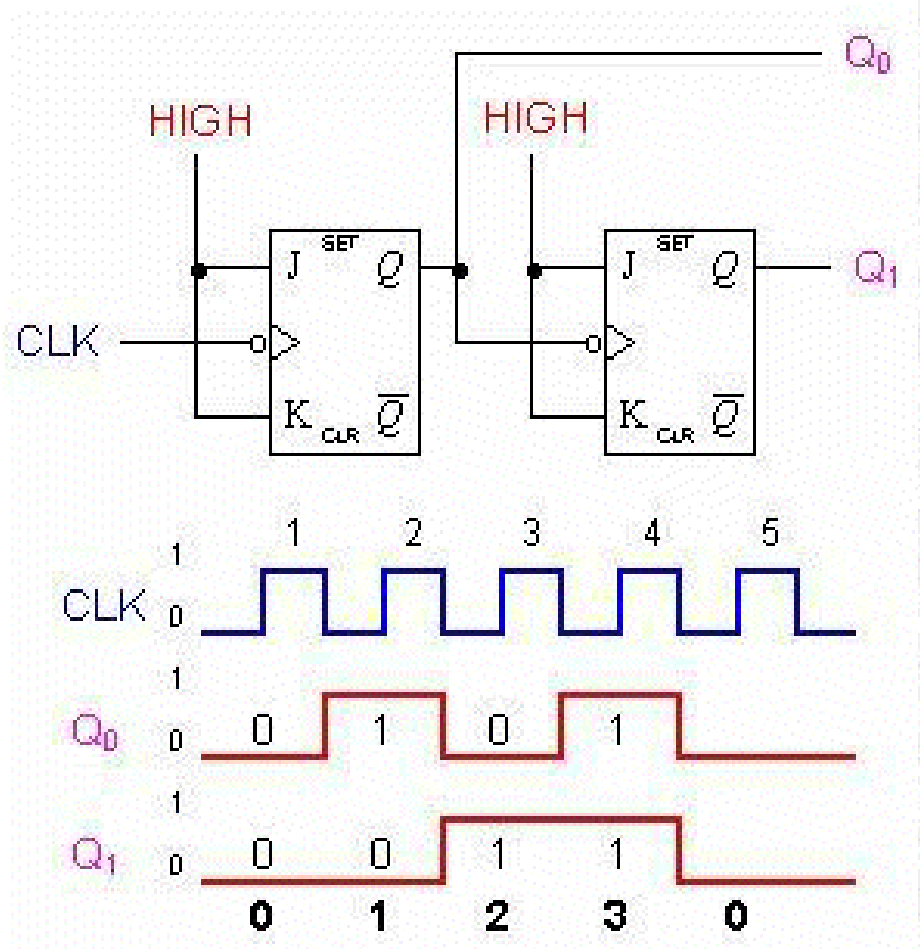
- The most typical uses of counters are
  - To count the number of times that a certain event takes place; the occurrence of event to be counted is represented by the input signal to the counter.
  - To control a fixed sequence of actions in a digital system.
  - To generate timing signals.
  - To generate clocks of different frequencies.
- Modulus (MOD) – the number of states it counts in a complete cycle before it goes back to the initial state.

INTRODUCTION TO COUNTERS

- Therefore, for n bit up or down counter, n number of flip-flop is required.
- The main characteristic of an asynchronous counter is each flip-flop derives its own clock from previous flip-flop and is therefore independent of the input clock.
- The output of the first flip-flop becomes the clock input for the second flip-flop, and the output of the second flip-flop becomes the clock input for the third flip-flop etc.
- For the first flip-flop, the output changes whenever there is a positive/negative transition in the clock input. This means that the output of the first flip-flop produces a series of square waves that is half the frequency of the clock input. Since the output of the first flip-flop becomes the clock of the second flip-flop, so the frequency of second flip-flop output is half the frequency of its original clock. This behaviour, in essence is captured by the binary bit pattern in the counting sequence

Asynchronous Counter

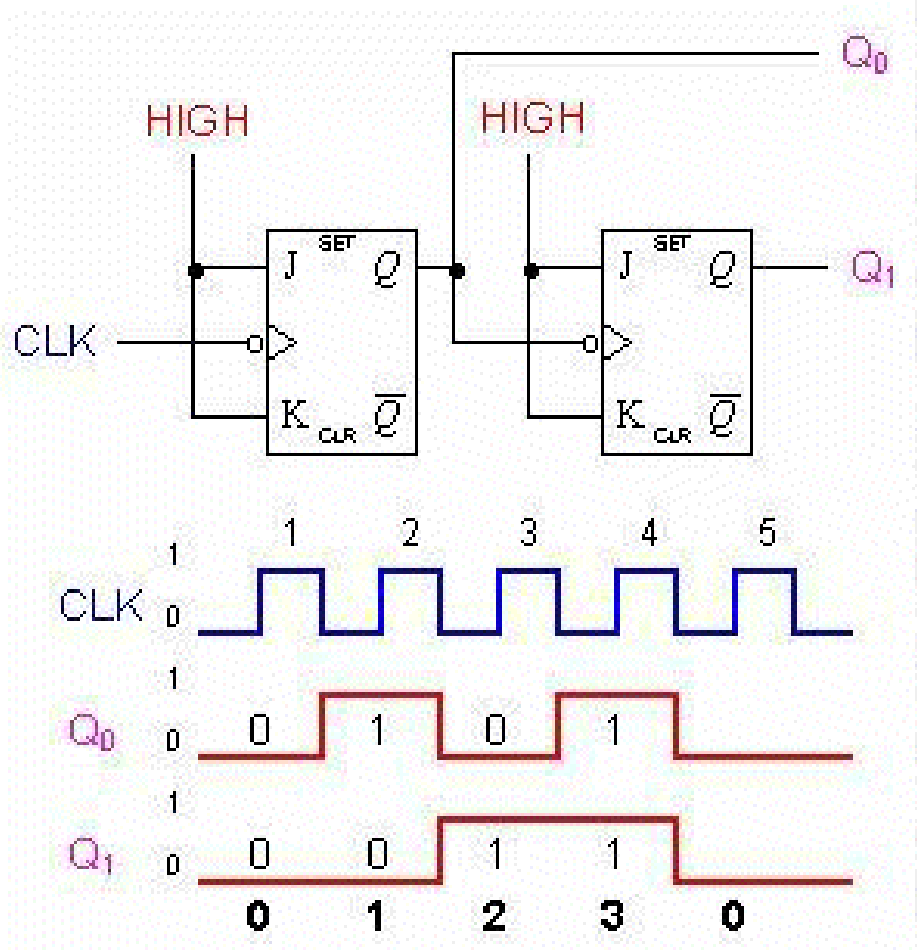
2 bit Binary Asynchronous up Counter



- A two-bit asynchronous counter is shown on the left. The external clock is connected to the clock input of the first flip-flop (FF_0) only. So, FF_0 changes state at the falling edge of each clock pulse, but FF_1 changes only when triggered by the falling edge of the Q output of FF_0.
- Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF_0 can never occur at exactly the same time. Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation.
- Although the transitions of Q_0, Q_1 and CLK in the timing diagram are shown as simultaneous, however, there are some small propagation delay between the CLK, Q_0 and Q_1 transitions. In real life circuit, this delay is insignificant to observe.

Asynchronous Counter

2 bit Binary Asynchronous up Counter

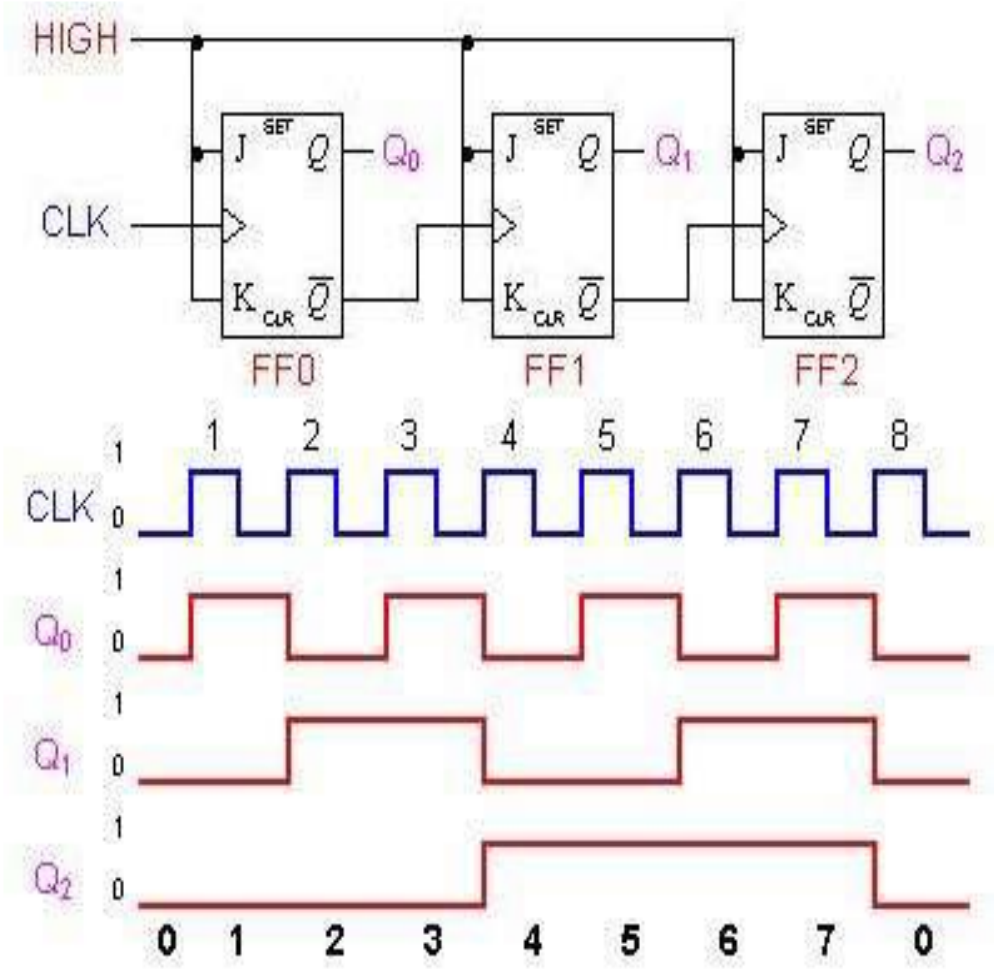


- Usually, all the CLEAR and SET inputs are connected together, so that a single pulse can clear all the flip-flops before counting starts. The clock pulse fed into FF_0 is rippled through the other counters after propagation delays, like a ripple on water, hence the name Ripple Counter.

- A mod-n counter may also be described as a divide-by-n counter. This is because the most significant flip-flop (the furthest flip-flop from the original clock pulse) produces one pulse for every n pulses at the clock input of the least significant flip-flop (the one triggers by the clock pulse). Thus, the above counter is an example of a divide-by-4 counter.

Asynchronous Counter

3 bit Binary Asynchronous MOD-8 up Counter

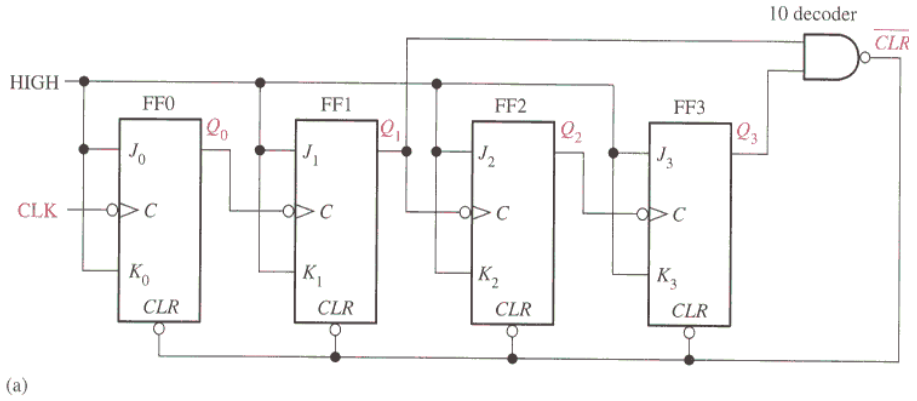


- A 3-bit asynchronous binary counter and its timing diagram is shown in the adjoining Fig.
- It works exactly the same way as a 2 bit asynchronous binary counter mentioned above, except it has eight states due to the third flip-flop.

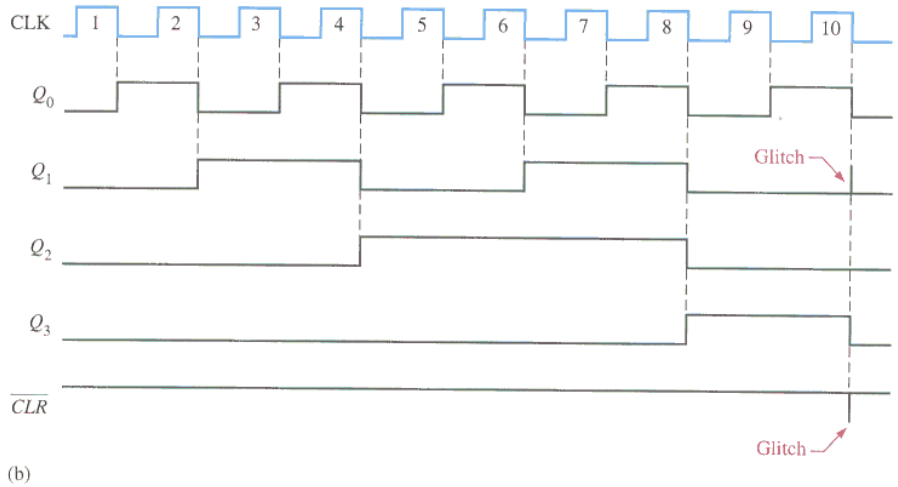
Clock Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

Asynchronous Counter

4 bit Binary Asynchronous Decade/MOD-10 up Counter



(a)

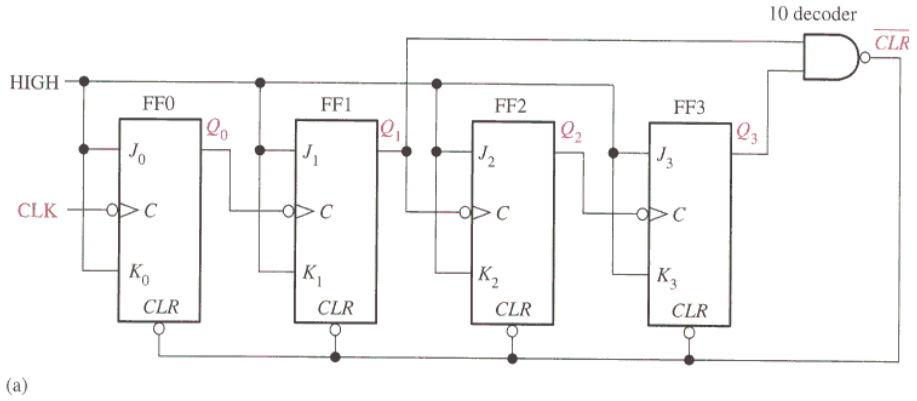


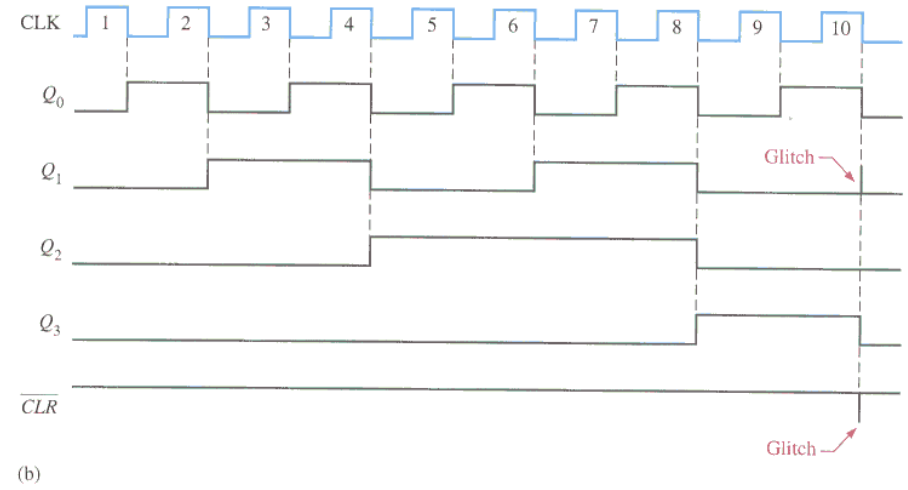
(b)

- The binary counters previously introduced have 2^n states. But counters with states less than this number can be designed to have the required number of states in their sequences and these are called truncated sequences. These sequences are achieved by forcing the counter to recycle before going through all of its normal states.
- A common modulus for counters with truncated sequences is ten and is called a decade counter.
- The required circuit diagram of a MOD-10 or Decade counter and its timing diagram is shown in the adjoining Fig.

Asynchronous Counter

4 bit Binary Asynchronous Decade/MOD-10 up Counter

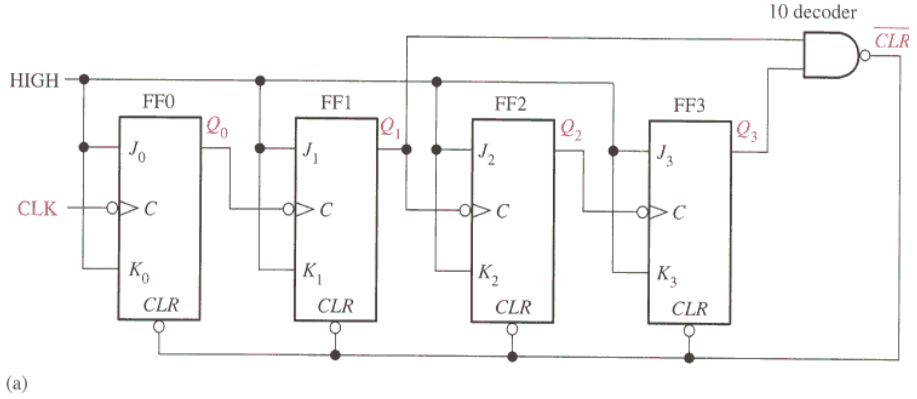


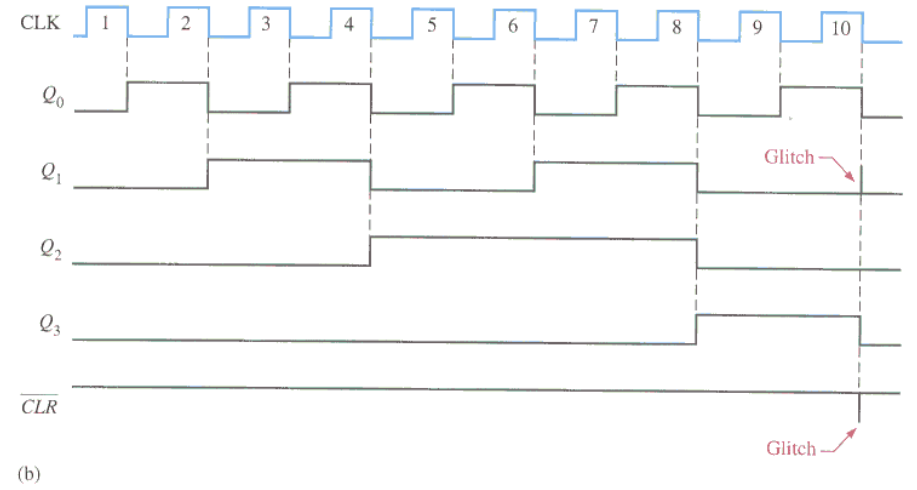


- The binary counters previously introduced have 2^n states. But counters with states less than this number can be designed to have the required number of states in their sequences and these are called truncated sequences. These sequences are achieved by forcing the counter to recycle before going through all of its normal states.
- A common modulus for counters with truncated sequences is ten and is called a decade counter.
- The NAND gate output becomes ‘0’ only when 1010 state comes. The ‘0’ output is applied in the CLR inputs of all flip-flops, resulting all the outputs become ‘0’. Therefore, after 1001 state, instead of 1010, the counter shows 0000 state.

Asynchronous Counter

4 bit Binary Asynchronous Decade/MOD-10 up Counter

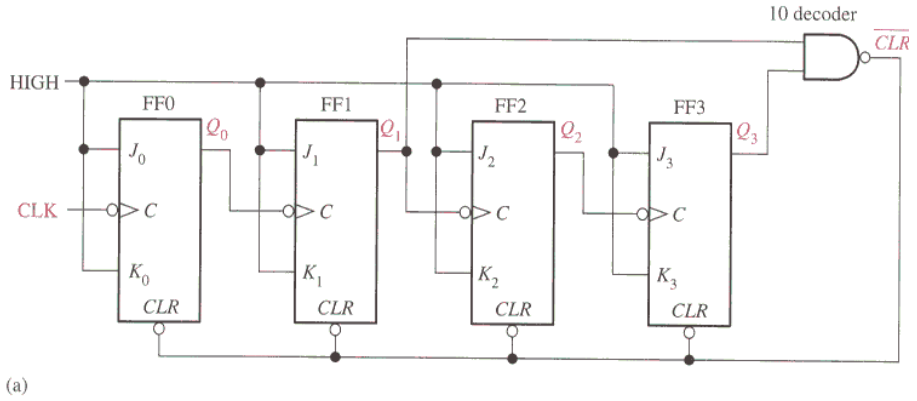




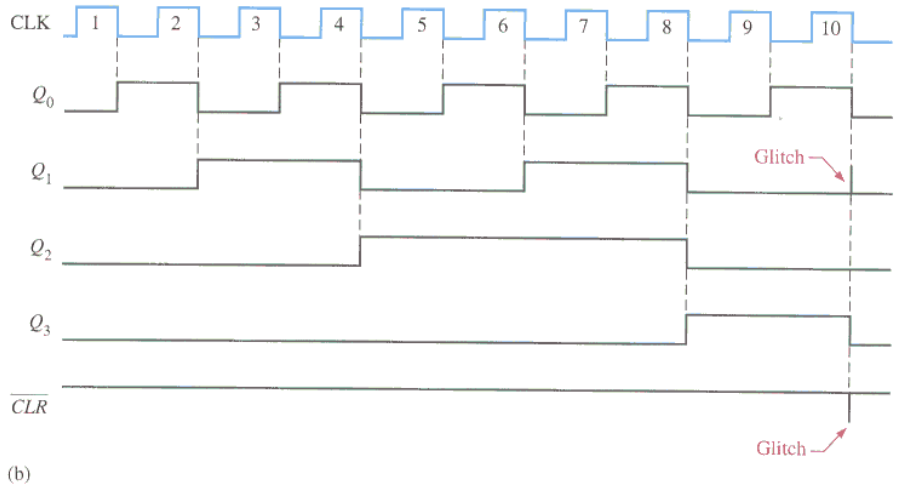
- The binary counters previously introduced have 2^n states. But counters with states less than this number can be designed to have the required number of states in their sequences and these are called truncated sequences. These sequences are achieved by forcing the counter to recycle before going through all of its normal states.
- A common modulus for counters with truncated sequences is ten and is called a decade counter.
- There is a glitch on the Q1 waveform. The reason for this glitch is that Q1 must first go HIGH before the count of 1010 can be decoded. Therefore, the counter is in the 1010 state for a short time before it is reset to 0000, thus producing the glitch on Q1 and CLR line that resets the counter.

Asynchronous Counter

4 bit Binary Asynchronous Decade/MOD-10 up Counter



(a)

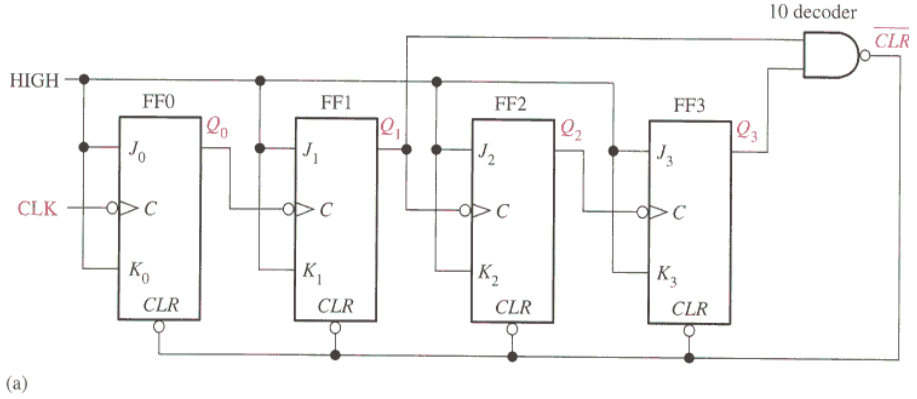


(b)

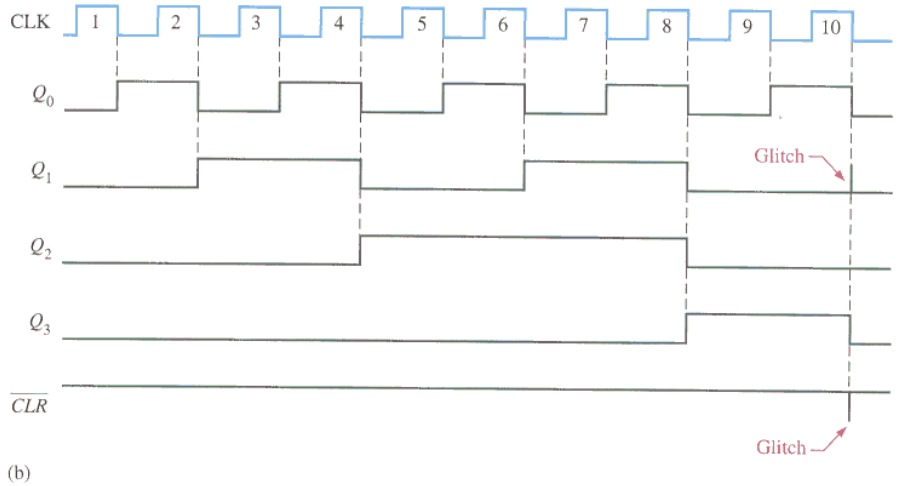
- The binary counters previously introduced have 2^n states. But counters with states less than this number can be designed to have the required number of states in their sequences and these are called truncated sequences. These sequences are achieved by forcing the counter to recycle before going through all of its normal states.
- A common modulus for counters with truncated sequences is ten and is called a decade counter.
- The operation of NAND gate happens so fast in real circuits, that the occurrence of 1010 state is not visible in naked eyes.

Asynchronous Counter

4 bit Binary Asynchronous Decade/MOD-10 up Counter



(a)

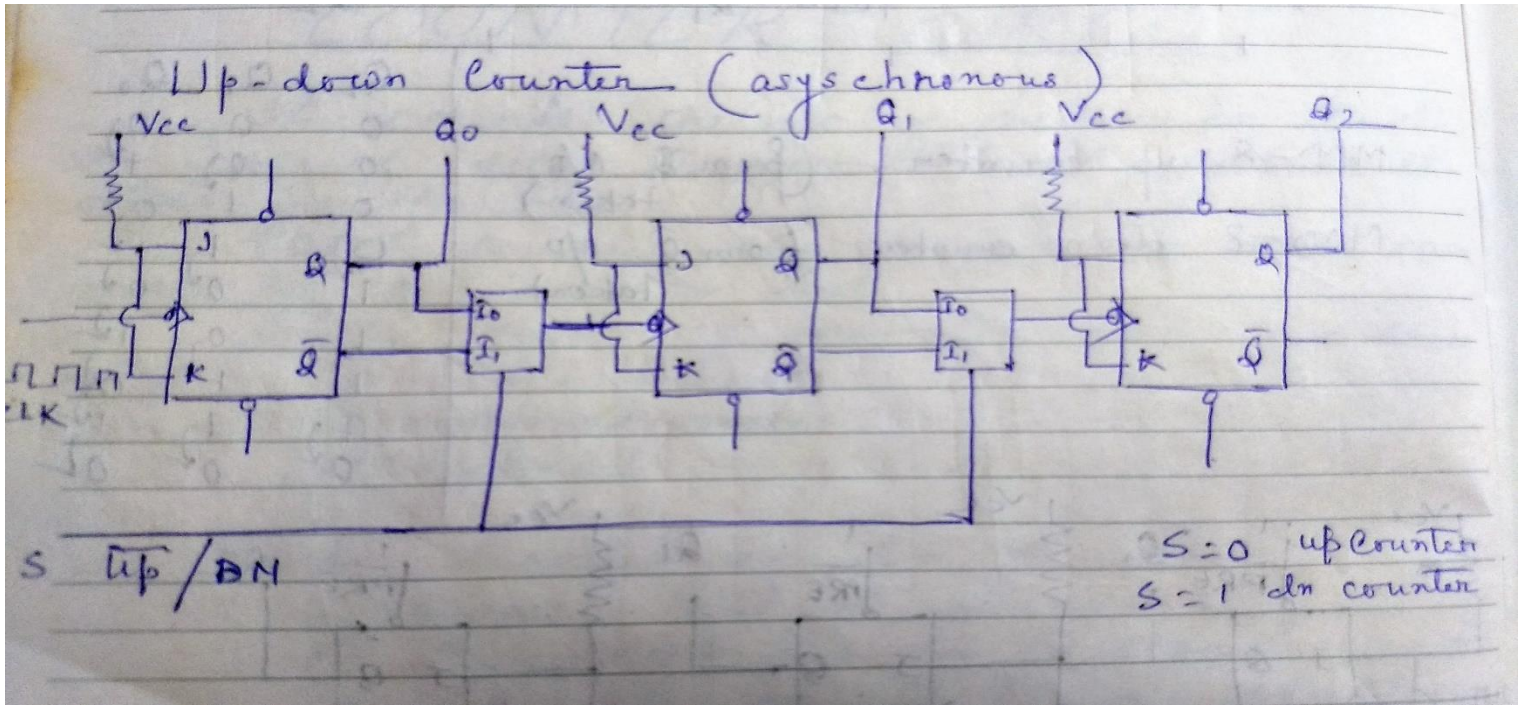


(b)

- The binary counters previously introduced have 2^n states. But counters with states less than this number can be designed to have the required number of states in their sequences and these are called truncated sequences. These sequences are achieved by forcing the counter to recycle before going through all of its normal states.
- A common modulus for counters with truncated sequences is ten and is called a decade counter.
- By using the same methodology, any other MOD-N truncated up or down counter can be designed.

Asynchronous Counter

3 bit Binary Asynchronous up/down Counter



- When the $\overline{\text{Up}}$/Dn control input is ‘0’, then I_0 of MUX inputs are selected, thus the next stage flip-flop gets clock input from Q output of previous stage and the circuit behaves as UP counter.
- When the $\overline{\text{Up}}$/Dn control input is ‘1’, then I_1 of MUX inputs are selected, thus the next stage flip-flop gets clock input from $\overline{Q}$ output of previous stage and the circuit behaves as DOWN counter.

Asynchronous Counter

ADVANTAGES:

- Asynchronous counters can be easily designed by T flip flop.
- These are also called as Ripple counters, and are used in low speed circuits.
- They are used as Divide by n counters, which divide the input by n, where n is an integer.
- Asynchronous counters are also used as Truncated counters. These can be used to designe any mod number counters, i.e. even Mod (ex. Mod 6) or odd Mod (ex. Mod 9).

DISADVANTAGES:

- Sometimes extra flip flop may be required for “Re-synchronization”.
- To count the sequence of truncated counters (mod is not equal to 2^n), we need additional feedback logic.
- While counting large number of bits, the propagation delay of asynchronous counters is very large.
- For high clock frequencies, counting errors may occur die to propagation delay.

For further information, go through the books of the following authors:

Digital Electronics:

- Diptiman Roy Chowdhuri (Vol. II)
- Salivanan
- Floyd
- Mano