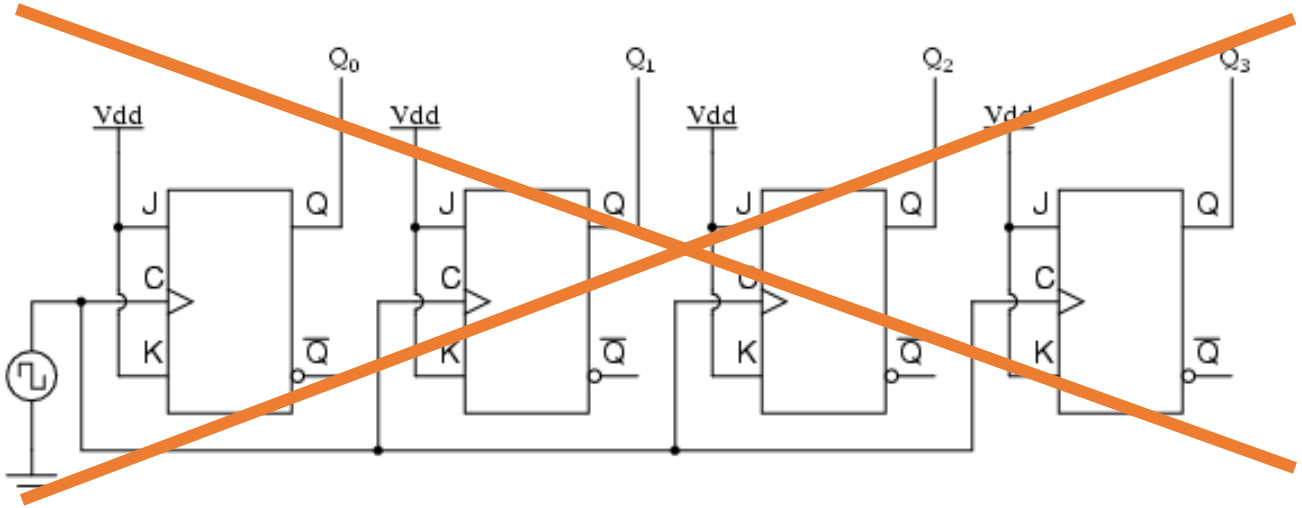
SYNCHRONOUS COUNTERS

- In the previous tutorial, we have learned about asynchronous counters. Though they are easily built, however there are several challenges.
- In synchronous counters, each and every flip-flop receives the exact same clock pulse at the exact same time. This means, the synchronous counter depends on the clock input to change their state value.
- There is no propagation delay and ripple effect in synchronous counters.

So, what do we do with the J and K inputs? Will the following circuit work?



NO!!!!!

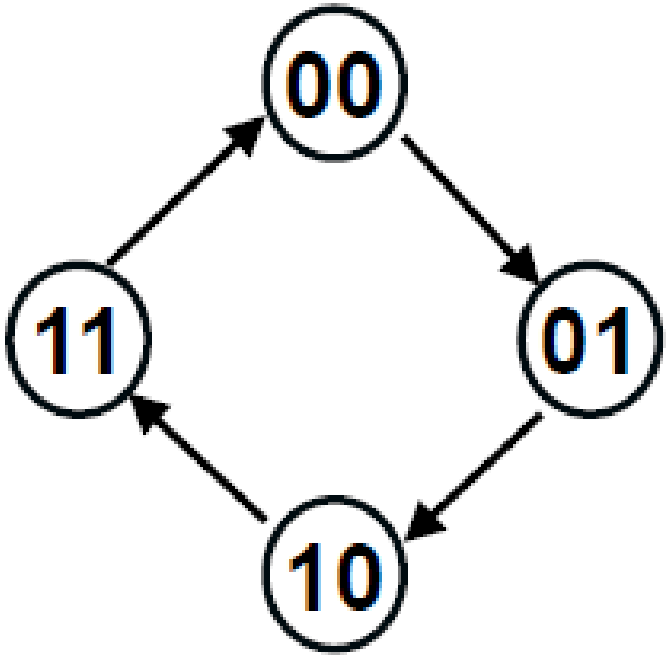
SYNCHRONOUS COUNTERS

- For synchronous counters, all the flip-flops are using the same CLOCK signal. Thus, the output would change synchronously.
- Procedure to design synchronous counter are as follows:
- **STEP 1:** Obtain the **State Diagram**.
- **STEP 2:** Obtain the **Excitation Table** using the state transition table for J-K FF and determine number of FF used.
- **STEP 3:** Obtain and simplify the function of each FF input **using K-Map**.
- **STEP 4:** Draw the **circuit**.

SYNCHRONOUS COUNTERS

Design a MOD-4 synchronous up-counter, using JK flip flop.

- **STEP 1:** Obtain the State transition Diagram



SYNCHRONOUS COUNTERS

Design a MOD-4 synchronous up-counter, using JK flip flop.

- **STEP 2:** Obtain the Excitation Table

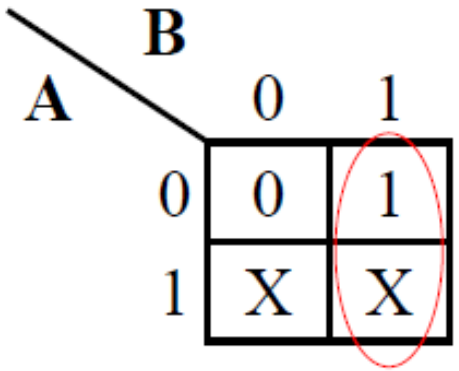
Present State	Next State	Input, J K	
B A	B A	J_B K_B	J_A K_A
0 0	0 1	0 X	1 X
0 1	1 0	1 X	X 1
1 0	1 1	X 0	1 X
1 1	0 0	X 1	X 1

NB: Please refer to "Digital Electronics by D. Roy Choudhuri" for better understanding of this step.

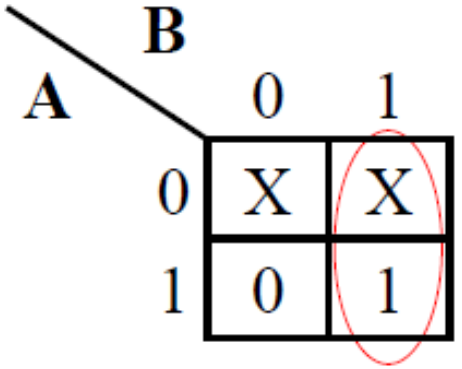
SYNCHRONOUS COUNTERS

Design a MOD-4 synchronous up-counter, using JK flip flop.

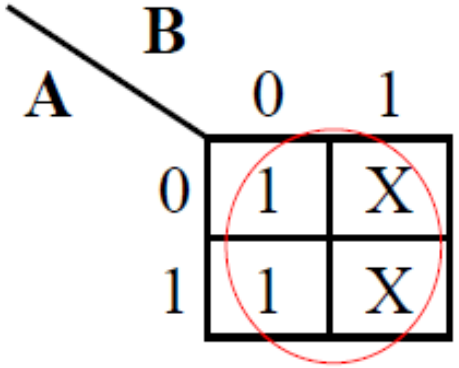
- **STEP 3:** Obtain the simplified expression for J and K from excitation table using K-Map



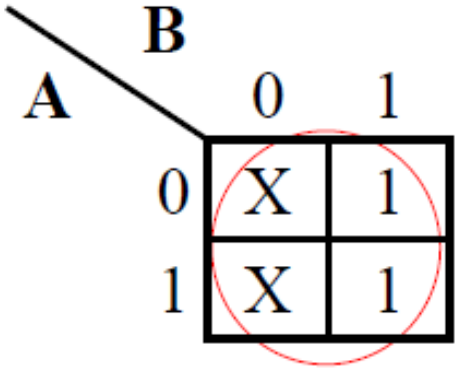
$J_B = A$



$K_B = A$



$J_A = 1$



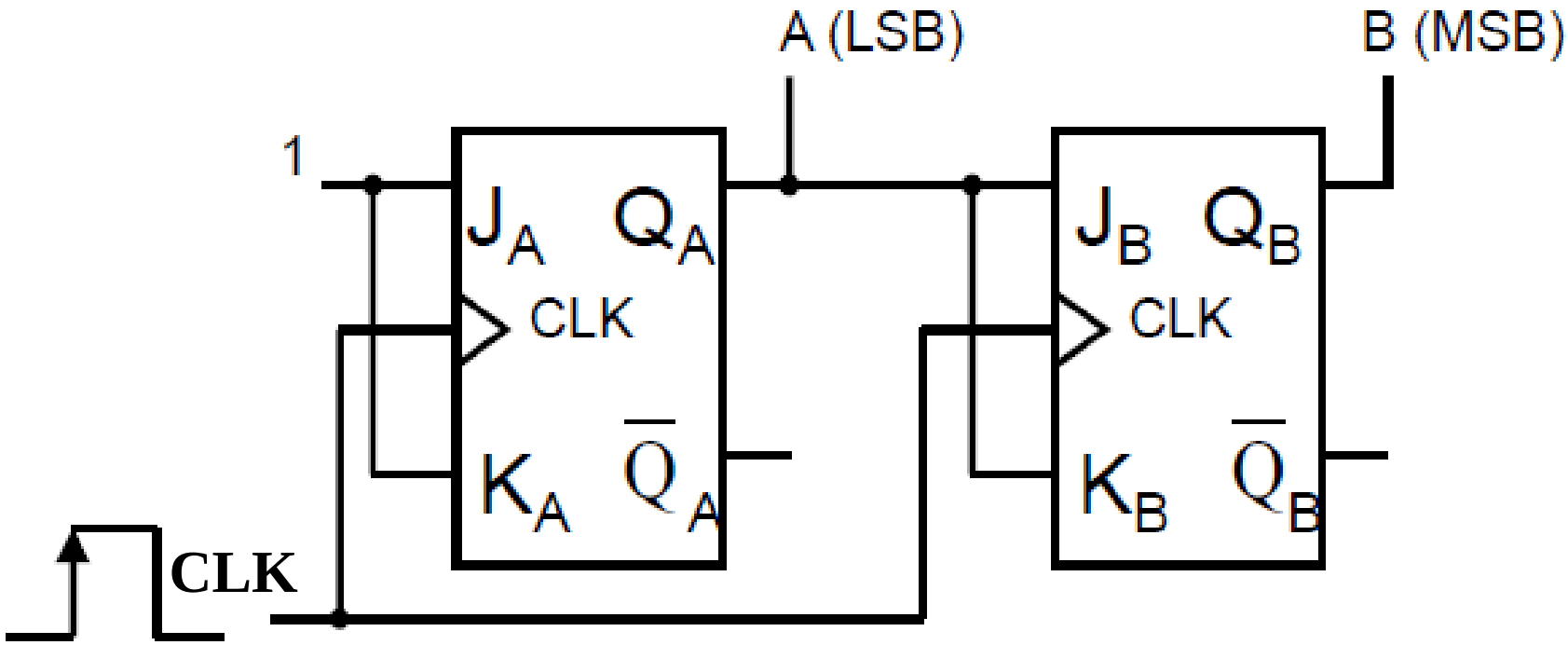
$K_A = 1$

NB: Please refer to "Digital Electronics by D. Roy Choudhuri" for better understanding of this step.

SYNCHRONOUS COUNTERS

Design a MOD-4 synchronous up-counter, using JK flip flop.

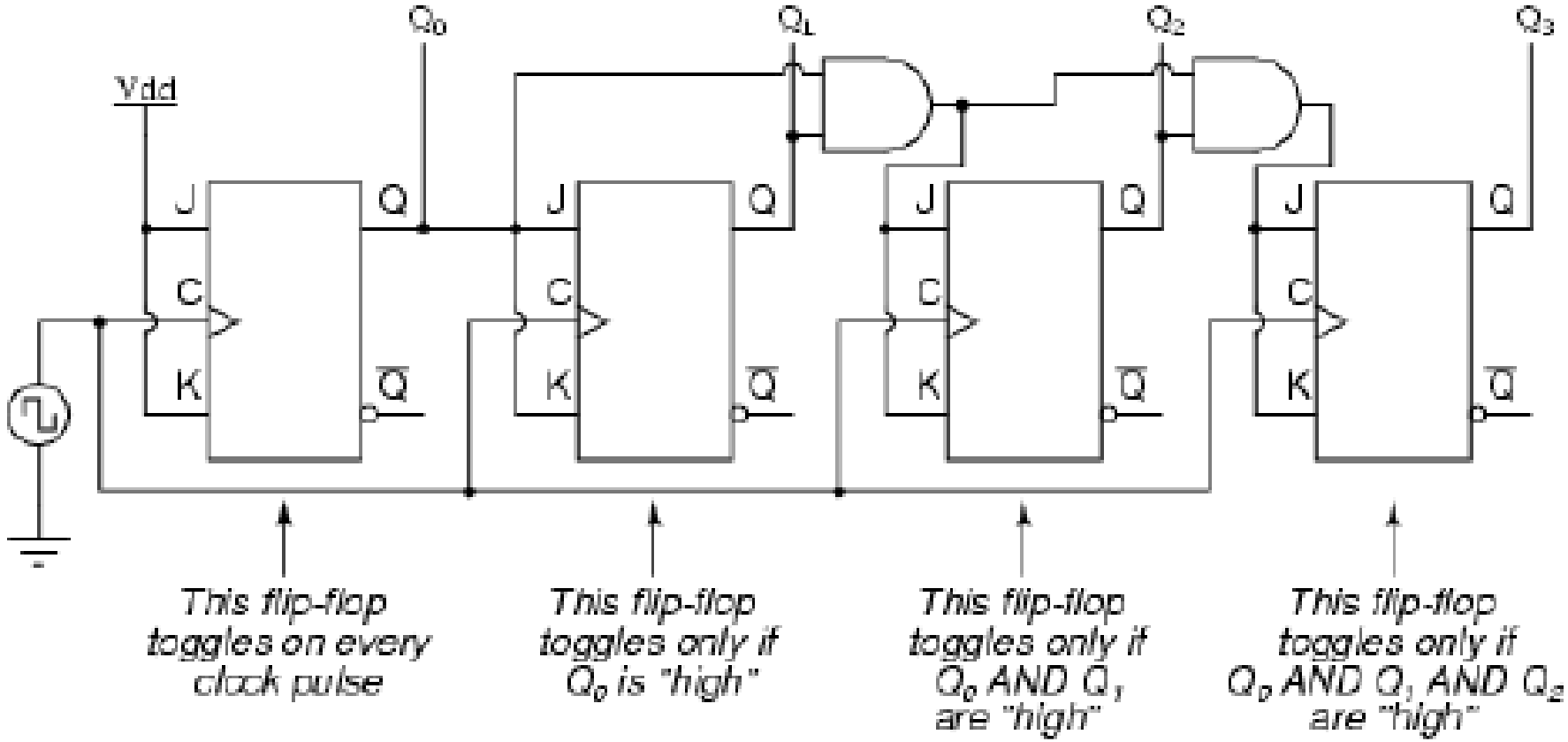
- **STEP 4:** Draw the circuit according to the obtained input expressions in STEP-3



SYNCHRONOUS COUNTERS

Design a MOD-16 synchronous up-counter, using JK flip flop.

- **By following the steps, MOD-16 synchronous up-counter can also be designed.**



SYNCHRONOUS COUNTERS

Design a MOD-16 synchronous up-counter, using JK flip flop.

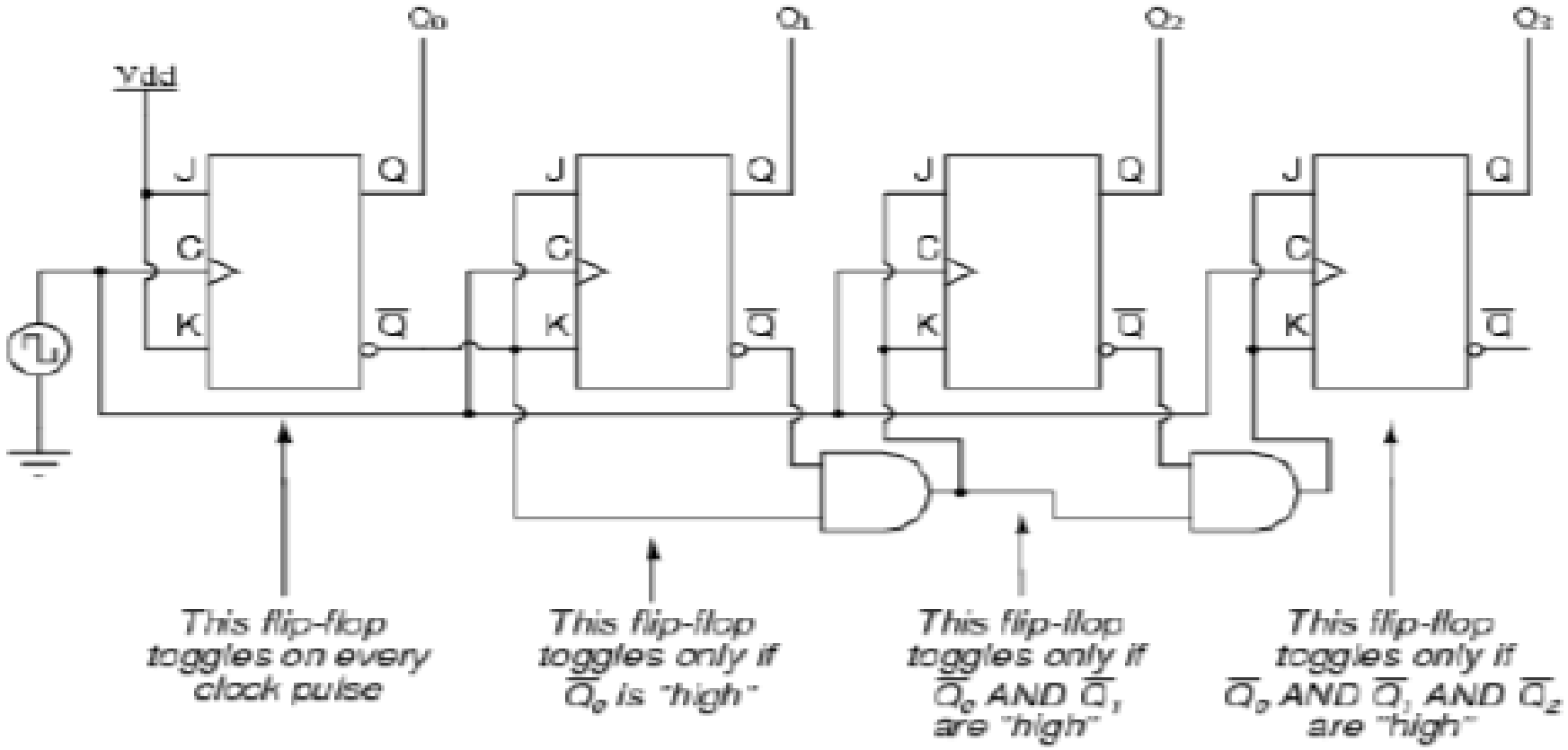
- **Working of this counter can be easily explained by using the following table:**

Clock pulse	Q4	Q3	Q2	Q1	Output	Output
1st Clock Pulse	Low	Low	Low	Low	0	0
2nd Clock Pulse	Low	Low	Low	High (starts toggling)	1	1
3rd Clock Pulse	Low	Low	High	Low	2	10
4th Clock Pulse	Low	Low (AND condition is not satisfied)	High (Remembers)	High	3	11
5th Clock Pulse	Low	High	Low (toggles)	Low	4	100
6th Clock Pulse	Low (AND condition not satisfied)	High (Remembers)	Low (remembers)	High	5	101
7th Clock Pulse	Low (AND condition satified)	High	High	Low	6	110
8th Clock Pulse	Low	High	High	High	7	111
9th Clock Pulse	High	Low	Low	Low	8	1000
10th Clock Pulse	High(Remembers)	Low	Low	High	9	1001
11th Clock Pulse	High	Low	High	Low	10	1010
12th Clock Pulse	High	Low	High	High	11	1011
13th Clock Pulse	High	High	Low	Low	12	1100
14th Clock Pulse	High	High	Low	High	13	1101
15th Clock Pulse	High	High	High	Low	14	1110
16th Clock Pulse	High	High	High	High	15	1111

SYNCHRONOUS COUNTERS

Design a MOD-16 synchronous down-counter, using JK flip flop.

- **Similarly, MOD-16 synchronous down-counter can also be designed by following the same steps.**



SYNCHRONOUS COUNTERS

Exercises:

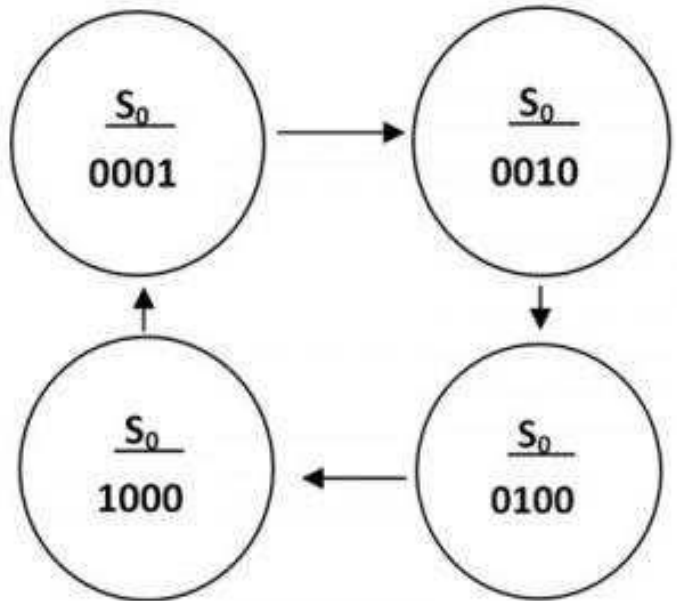
- **Design a synchronous counter to count in the following sequence:**
  6, 4, 3, 1, 6, 4, 3, 1, 6 …

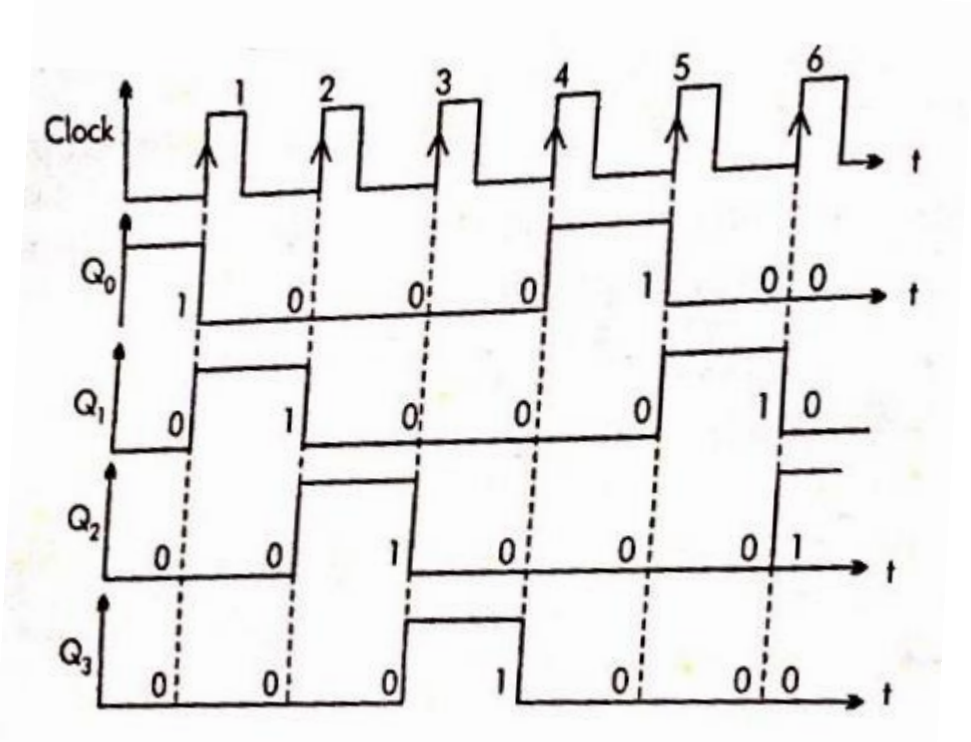
- **Design a synchronous counter to count in the following sequence:**
  1, 3, 5, 7, 1, 3, 5, 7, 1 …

- **Design a synchronous counter to count in the following sequence:**
  1, 5, 3, 4, 1, 5, 3, 4, 1 …

RING COUNTER

- The ring counter is a cascaded connection of flip-flops, in which the output of the last flip flop is connected to the input of the first flip flop.
- This counter is designed using serial-in-serial-out/parallel-out shift register.
- The ring counter is not used for counting a sequence, but rather as a timing sequence generator.
- The state diagram and timing diagram for ring counter is shown below:





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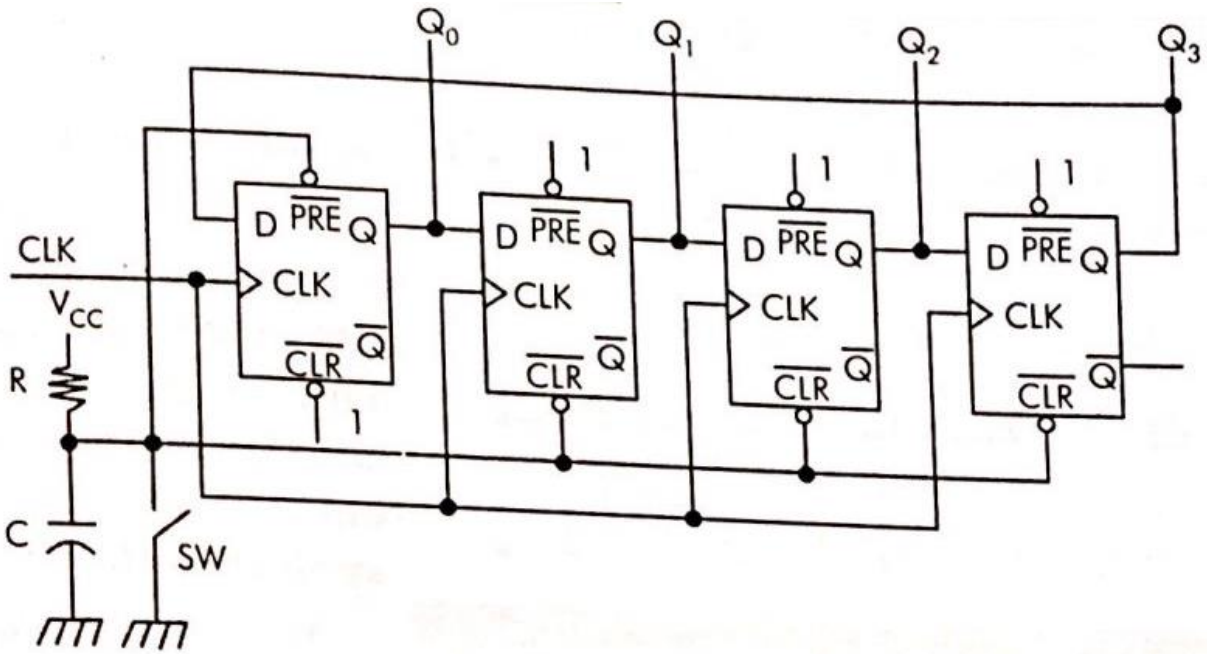
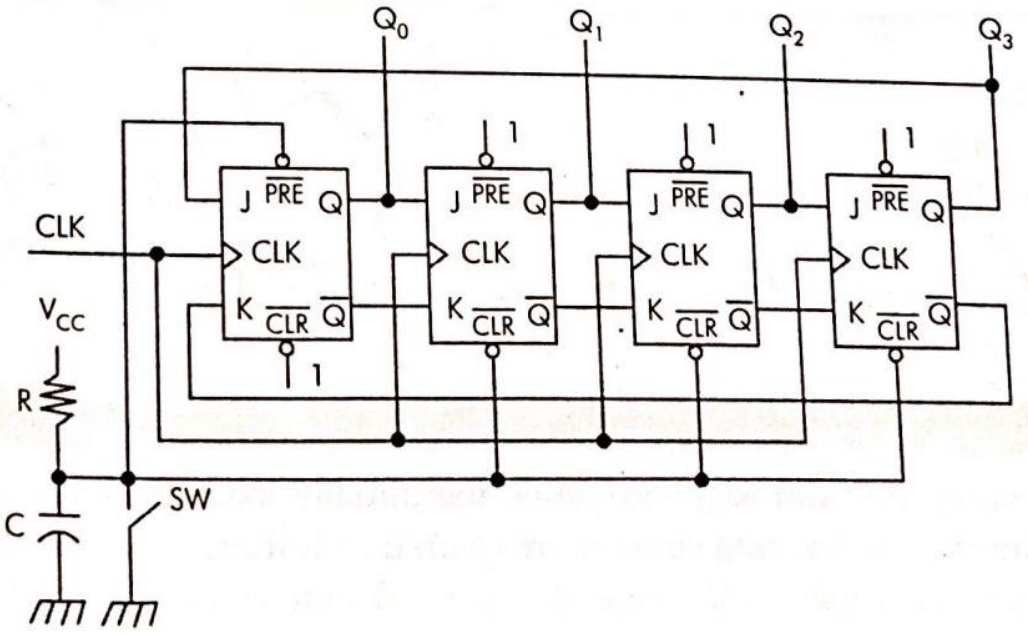
- The ring counter is not used for counting a sequence, but rather as a timing sequence generator.
- The **<u>circuit diagrams using D- and J-K flip flops</u>** for ring counter are shown below:



Ring Counter using D- Flip Flop

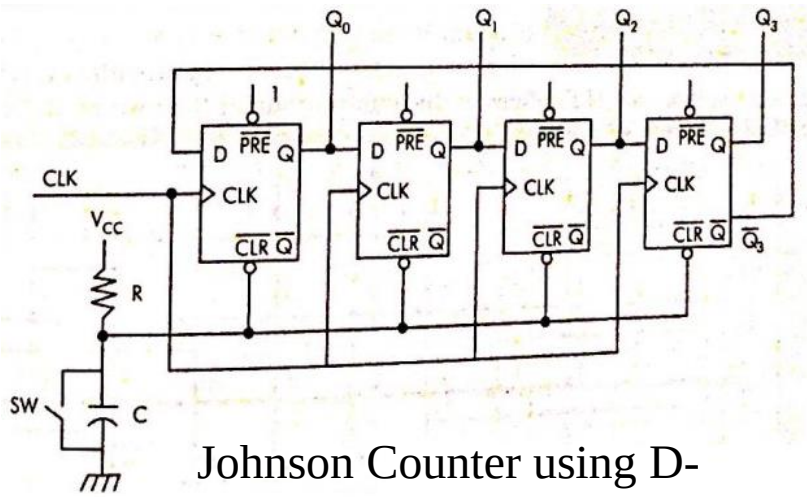


Ring Counter using J-K Flip Flop

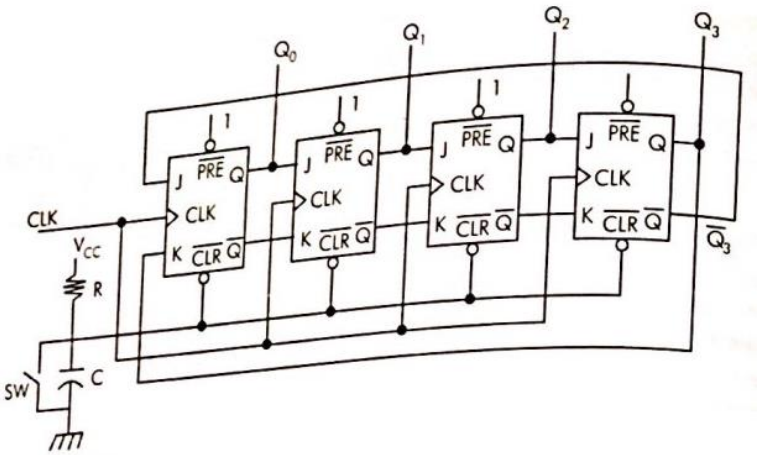
JOHNSON COUNTER

- The Johnson counter is similar to Ring counter, except in ring counter the output of the last flip flop is directly connected to the input of the first flip-flop. But in Johnson counter, the inverted output ($\bar{Q}$) of the last flip-flop is connected to the first flip flop input.
- For circuits with JK flip-flop, connections are made from $\overline{Q_n}$ and Q_n of the last flip flop to the J and K input of first flip flop.
- For 4-bit Johnson counter, the output may start from either 1111 or 0000, unlike 1000 output for ring counter.
- The counter output sequence and circuit diagram is shown below:

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
repeat			



Johnson Counter using D-Flip Flop



Johnson Counter using JK-Flip Flop

For further information, go through the books of the following authors thoroughly:

Digital Electronics:

- Diptiman Roy Chowdhuri (Vol. II)
- Salivanan
- Floyd
- Mano